# ISL6752/54EVAL1Z ZVS DC/DC Power Supply with Synchronous Rectifiers User Guide

The ISL6752/54EVAL1Z is a new design based on the ISL6752EVAL1Z but with several design modifications to improve the efficiency from 90% to 95%. The control circuit has been moved off the main board onto a daughter card. Two different daughter cards are provided: one using the ISL6752 and the other using the ISL6754. Both control cards utilize the Intersil zero voltage switching (ZVS) topology. The ISL6752 daughter card features pulse by pulse current limiting, and the ISL6754 daughter card features a patented method for average current limiting that results in a brick-wall current limit profile.

The PCB layout of the ISL6752/54EVAL1Z has also been greatly improved over the ISL6752EVAL1Z. Even though the overall size of the board has been reduced, the copper losses have been reduced.

In addition to the ZVS function, this board also incorporates N-Channel FETs as secondary side rectifiers, also known as synchronous rectifiers (SR). Power dissipation of the secondary side rectifiers is reduced because the conduction losses of SRs are significantly less than the conduction losses of PN or Schottky diodes.

## Scope

This application note covers implementation of synchronous rectifiers (SRs) and their associated drive circuits as used on the ISL6752/54EVAL1Z board. Implementation of the primary side ZVS controller, based on the ISL6752 daughter card, is described extensively in Intersil Application Note AN1262, "Designing with the ISL6752, ISL6753 ZVS Full-Bridge Controllers."

Also reviewed is the performance of this evaluation board. Oscillographs illustrate the performance of the power supply with load transients on the output. The ZVS switching of the bridge FETs is shown, and efficiency and load regulation are measured.

At the end of this application note, the schematics, bill of materials, and printed circuit board layouts are included for reference.

### TABLE 1. SPECIFICATIONS

| Absolute Maximum Input Voltage | 450VDC |
|---|---|
| Operating Input Voltage | 350V to 450VDC |
| Maximum Input Current | 2.5ADC |
| Rated Output Current | 50ADC |
| Current Limit | 60A ± 5% |
| Output Voltage | 12V ± 5% |
| Efficiency at 100% (50A) Load | 95% |
| Efficiency at 20% (10A) Load | 92% |



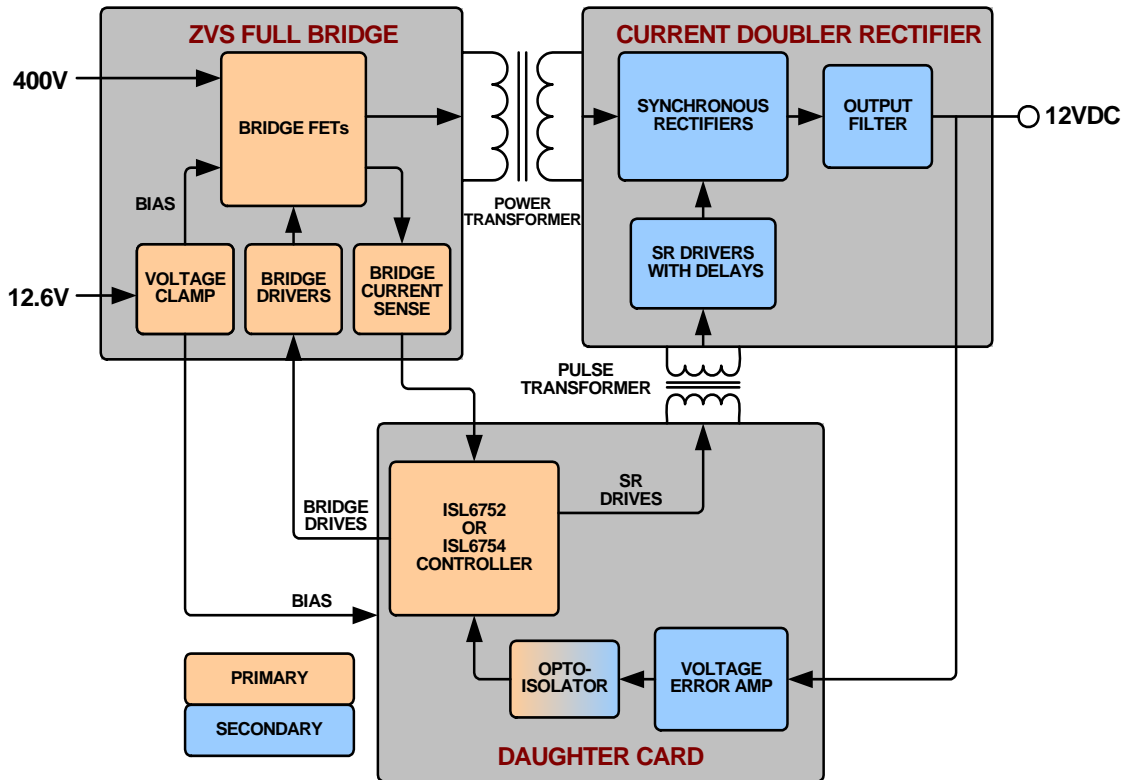**FIGURE 1. NEW ISL6752/54EVAL1Z**

**FIGURE 2. ISL6752/54EVAL1Z BLOCK DIAGRAM**

# Block Diagram

The evaluation board is composed of several distinct circuit elements. The three main sections are the ZVS full bridge on the input, the current doubler rectifier on the output, and the controller daughter card. See "Schematics- Main Board, ISL6752/54EVAL1Z" on page 23 and "Schematics - Daughter Card" on page 25 for complete circuit details.

## Daughter Cards

The ISL6752 or ISL6754 control ICs are located on their respective daughter cards, as shown in Figures 3 and 4. Both daughter cards have the control ICs on the primary side and the voltage error amplifier on the secondary side. Creepage spacing between the primary and secondary is maintained on the cards.

The ISL6752 and the ISL6754 control ICs are located on the primary side, eliminating the need for two AC line isolating gate drive transformers to drive the primary side bridge FETs. Instead, the low side FETs are driven directly by MOSFET drivers (on the main board), and the high side FETs are driven by a gate drive transformer that only requires operational insulation. Primary side control also simplifies design of the current sensing transformers because they also do not have to be AC line isolating.

A line isolation rated opto-coupler (D5 on ISL6752DB or D2 on ISL6754DB) passes the analog error signal generated by the error amplifier, U1, from the secondary to the primary. Opto D3 passes a digital signal from primary to secondary to turn off the SRS for diode emulation.

The only functional difference between the ISL6752 and ISL6754 daughter cards is how current limit is implemented. The ISL6752 uses pulse-by-pulse current limit, and the ISL6754 uses average current limit.
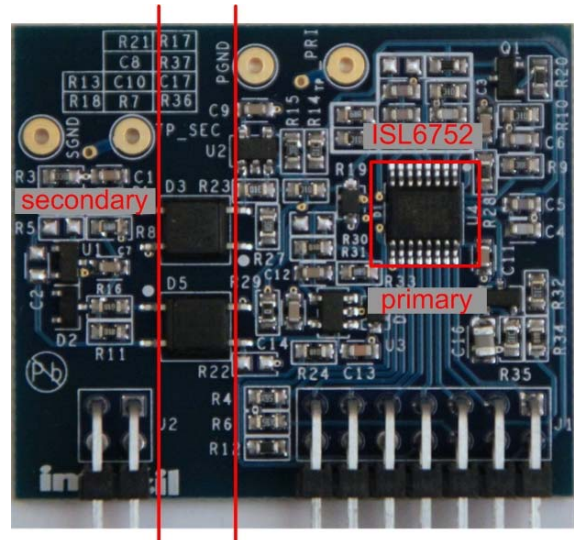


**FIGURE 3. ISL6752 DAUGHTER CARD**

Special test points located on the daughter cards aid in probing nodes on the daughter cards for evaluation. Test points PGND and TP_PRI are located on the primary side, and SGND and TP_SEC are located on the secondary. With these test points, the user can employ the spring-like probe accessories included with

many scope probes. The scope signal pin is inserted in TP_PRI (or TP_SEC), and the short spring ground lead is inserted in PGND (or SGND).
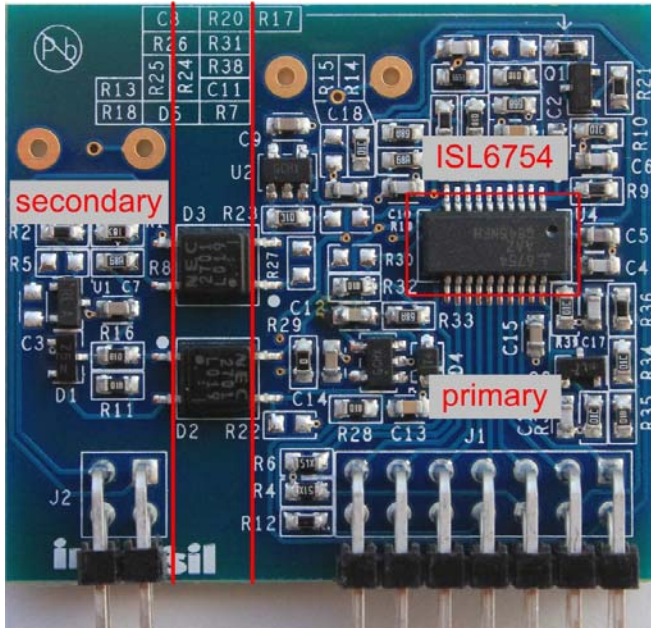


FIGURE 4.  ISL6754 DAUGHTER CARD

To probe any node on the daughter card, solder a 30ga insulated wire between the desired node and the via that is associated with the TP_PRI or TP_SEC test point. This method not only simplifies probing of any node, but also implements the preferred technique of measuring small signals in the presence of high amplitude switching magnetic fields.

The ISL6752DBEVAL1Z and the ISL6754DBEVAL1Z daughter cards are also available as standalone evaluation kits.

## ZVS Full Bridge

The low side FETs, $Q_3$ and $Q_4$, are driven directly by the ISL89160 MOSFET driver, U1 (Figure 5). The two high-side FETs, $Q_1$ and $Q_2$, are indirectly driven by the ISL89160 driver, U2. A level translating gate drive transformer, $T_3$, with complementary output windings, directly drives the high-side bridge FETs with a symmetrical square wave. The design of $T_3$ is simplified because it only needs 400V operational insulation, and it is always driven with a square wave, thus eliminating the problems associated with non-symmetrical drive waveforms.

Observe that the ISL89160 MOSFET drivers are located as close as possible to their respective bridge FETs to minimize the detrimental effects of parasitic inductance on the outputs of the drivers. Although the input signal lead lengths between the drivers and the daughter card are relatively long (about 5cm), they are shielded on top and bottom by ground planes, to significantly reduce the noise injected on these lines. The hysteresis of the ISL89160 inputs also lessens the possibility of noise corrupting the gate signals.
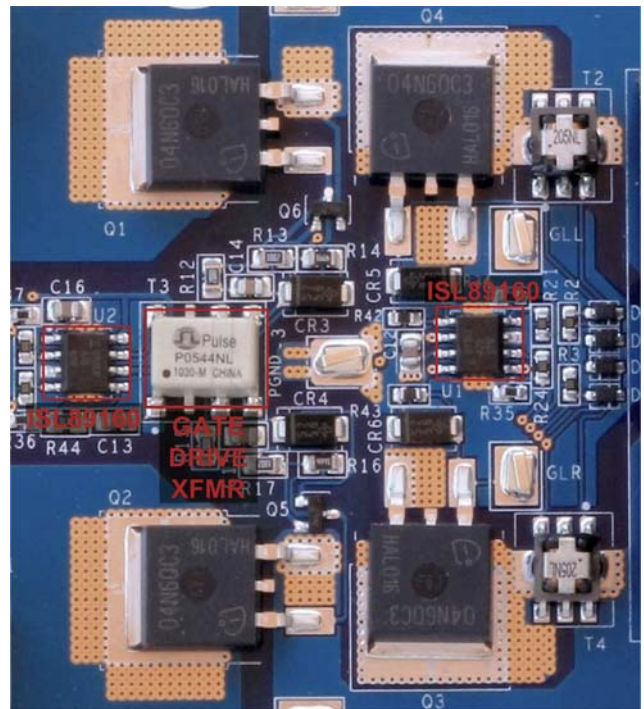


FIGURE 5.  FULL BRIDGE

## High Voltage Protection

Because a failure of the bridge can cause catastrophic damage to the primary side control elements, a voltage crowbar, F1 and $D_3$, and a voltage blocking diode, $D_4$, are incorporated (Figure 6). $D_3$ clamps the bias voltage to a safe level. If 400V is applied to the $V_{DD}$ node, F1 opens shortly after $D_3$ conducts current. $D_4$ provides additional protection by blocking high voltage from being applied to the 13V lab supply. Note that a fully debugged power supply does not need these additional components. These parts are included on the evaluation board to minimize damage, should the user accidently introduce a fault while evaluating the circuits. The designer may want to keep F1 in the final design, to prevent a loud bang if the bridge does fail.
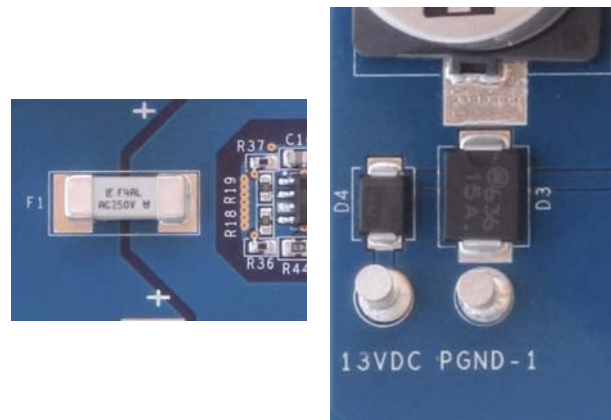


FIGURE 6.  PROTECTION CIRCUITS

## Primary Side Current Sensing

The primary side bridge has two current sensing transformers, $T_2$ and $T_4$, one on each leg on the drains of the low-side bridge FETs (Figure 7). Using two transformers allows each CT to reset during alternate half cycles. Alternate current sensing methods are reviewed in "Current Sensing" on page 8.
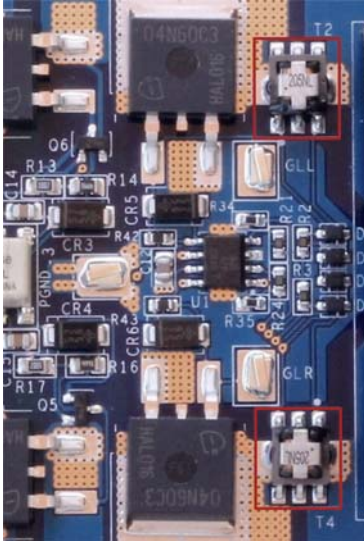


FIGURE 7. PRIMARY SIDE CURRENT SENSING

## Synchronous Rectifier Drive Circuit

Two banks of SRs are driven by the ISL89163 MOSFET driver, U4 (Figure 8). An RCD network on the inputs to this driver delay the turn-on of the SRs relative to the turn-off of the primary side bridge FETs.

The ISL89367, U108, can optionally be used to drive the SRs instead of the ISL89163. Review "Schematics - Daughter Card" on page 25 to understand how to disconnect the ISL89163 and connect the ISL89367.

The pulse transformer, $T_6$, crosses the isolation boundary to couple the control signals from the ISL6752, ISL6754 to the MOSFET drivers (Figure 9). Note that this transformer also provides the secondary side bias voltage for the MOSFET drivers.
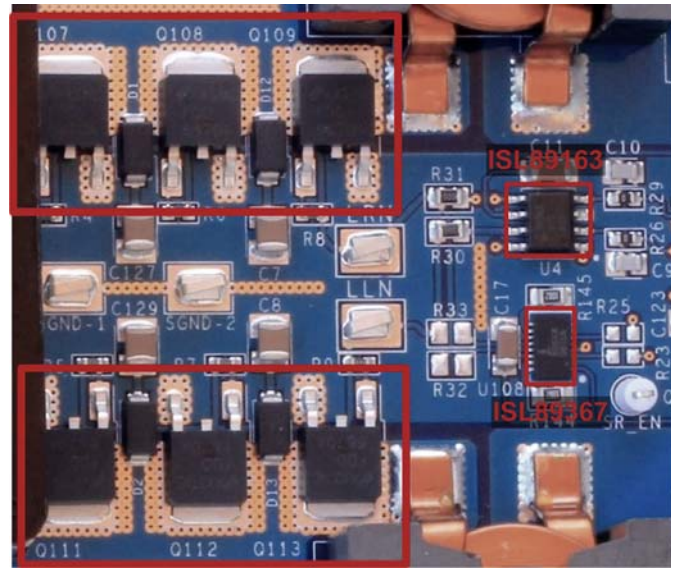


FIGURE 8. SRs AND DRIVERS



FIGURE 9. PULSE TRANSFORMER AND DRIVER

## Current Doubler Output

The current doubler output is composed of two banks of SRs, $Q_{107}$... $Q_{109}$ and $Q_{111}$... $Q_{113}$; inductors $L_{102}$ and $L_{103}$; and output filter capacitors, $C_{133}$... $C_{136}$ (Figure 10). The advantage of this topology is that the output current is shared by the two inductors, thus reducing conduction losses. Another advantage is that the secondary winding of the power transformer does not require a center tap.
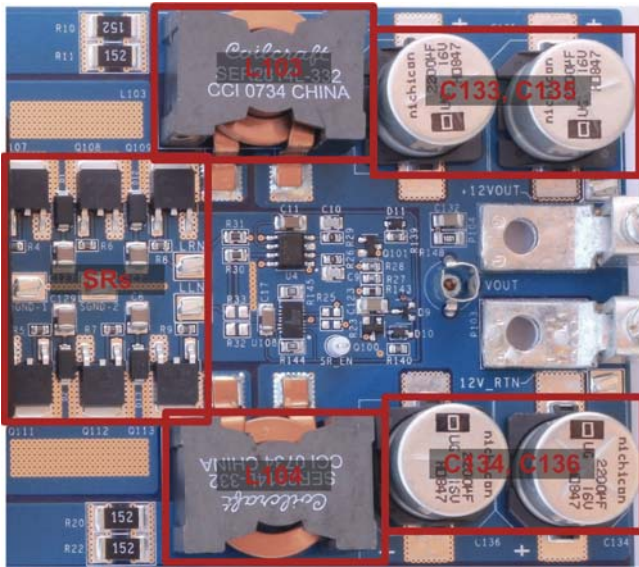
**FIGURE 10.  CURRENT DOUBLER OUTPUT**

# Basic SR Principles

Replacing diodes with MOSFETs has two major advantages:

- Dramatically reduces conduction losses
- The applied duty cycle remains virtually constant from no load to full load.

Disadvantages are:

- Additional complexity and cost

- Higher reverse recovery losses as compared to fast recovery diodes.

- When paralleling units for redundancy, provisions must be made to prevent current circulation among the paralleled units.

## SR Drive Timing Requirements

To emulate a diode, an SR must be driven ON when a diode would normally be conducting. But unlike a diode, if the SR is ON, the current through the SR can reverse if the voltage on the SR "cathode" becomes positive. The consequence is that if the SR is driven ON when the primary side is sourcing voltage to the secondary, the secondary side will be shorted by the SR.

Figure 11 illustrates the timing required to drive the SRs. Note that the rising edges of the two lower bridge FETs are delayed by the ISL6752/54 relative to the PWM signal. Likewise, the rising edges of the SRs gate signals are delayed by the ISL89163 relative to the falling edge of the PWM signal. These delays are necessary to prevent the overlap of drive signals that would result with high amplitude short circuit currents.

When an SR is turned off while current is flowing from source to drain, the current diverts from the FET channel to the internal body diode. Because the voltage drop across the body diode is higher than the channel, it is desirable to minimize dissipation by minimizing the duration of the current flow through the body diode.
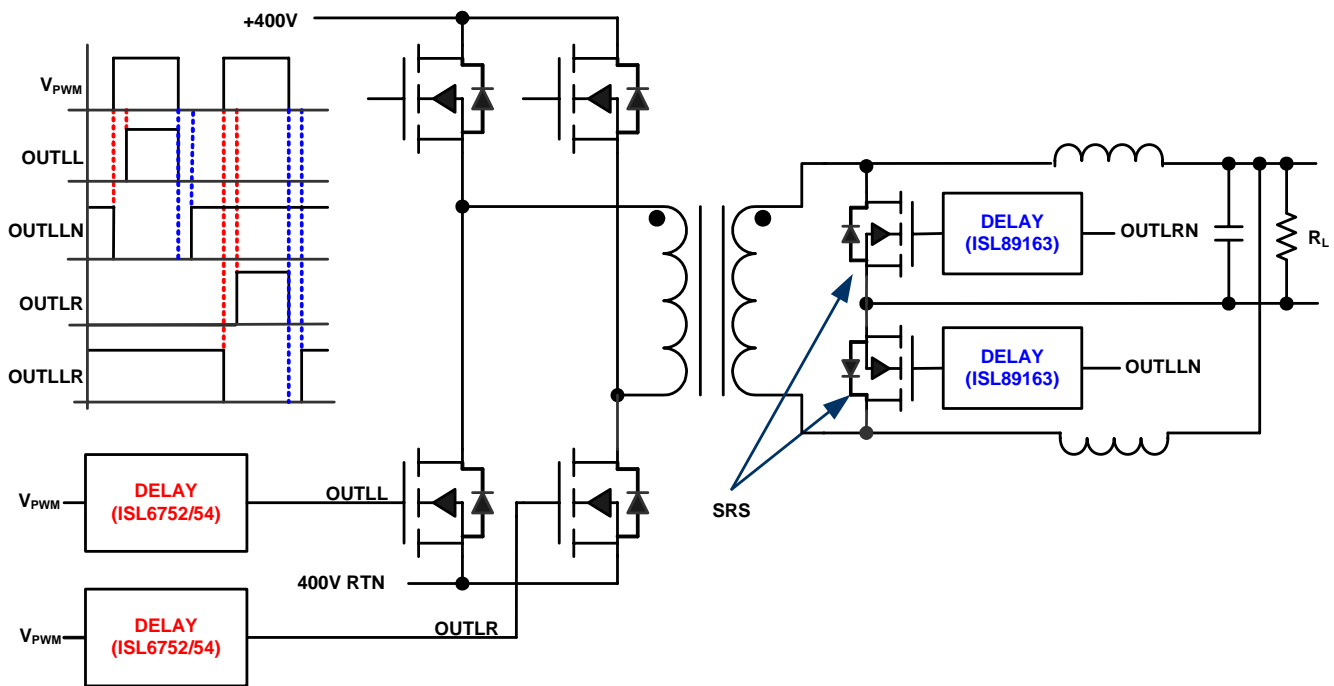


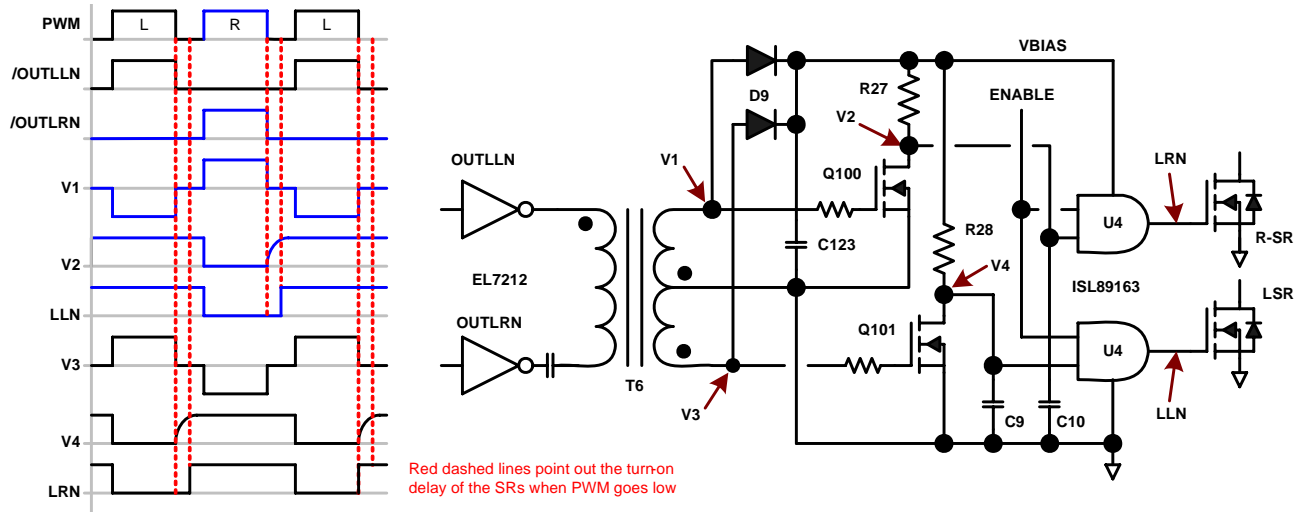**FIGURE 11.  TIMING FOR SRs AND BRIDGE FETs**

FIGURE 12. SIMPLIFIED SR DRIVE SCHEMATIC

## SR Drive and Bias

OUTLLN and OUTLRN in Figure 12 are control signals from the ISL6752/54 that are used to drive the SRs. Because the ISL6752/54 is located on the primary side, a pulse transformer, $T_6$, is used to cross the isolation boundary. The simplified schematic of Figure 12 illustrates the use of $T_6$ to not only couple OUTLLN and OUTLRN to the secondary, but also to generate the bias for drivers on the secondary.

When /OUTLLN or /OUTLRN (outputs of EL7212) transitions to a logic high, it is necessary to turn off the associated SR quickly. For example, when /OUTLRN (blue) transitions high, V1 is high, and C10 is quickly discharged by Q100. U4 then drives R-SR off. In a similar manner, when /OUTLLN is high, U4 drives L-SR off.

When /OUTLLN or /OUTLRN transitions to a logic low, it is necessary to turn on the SRs after a time delay, to prevent the SRs from shorting the primary side bridge when it is sourcing current. For example, when /OUTLRN transitions to low, V1 is low and Q100 turns off, allowing C10 to be charged by R27. When the positive threshold of UR is exceeded, the output of U4 drives on R_SR. In a similar manner, the high to low transition of /OUTLLN results in the output of U4 driving on L_SR after a time delay.

Note that the cathodes of D9 are connected together to peak charge C123. Because C123 is large in value, after the initial charging, the voltage does not change significantly from cycle to cycle. An important aspect of generating the bias for U4 in this manner is that the thresholds for the logic transitions on the inputs of U4 are proportional to VBIAS, and the voltage to charge C9 and C10 is also VBIAS. Consequently, the delays generated by the RC networks are independent of the absolute value of VBIAS.

## Current Doubler

Figure 13 illustrates the current flow in the two inductors of the current doubler topology. Current flow in the circuit is correlated with the waveforms by color coding. The green waveform represents the sum of red and blue currents through $R_{LOAD}$. For circuit clarity, paralleled SRs and output capacitors of the ISL6752/54EVAL1Z board are not shown.

When using diodes (instead of SRs), if the average load current is less than half of the ramp current in the output inductors, the current in the inductors becomes discontinuous, and the duty cycle of the PWM is shortened to maintain the desired output voltage.

When using SRs, the inductor currents in $L_1$ and $L_2$ can become negative because current in SRs can flow bidirectionally; consequently, the duty cycle remains virtually unchanged. The benefit is that the load transient performance is the same for any load from zero up to current limit. Another advantage is that, for very light loads, the duty cycle is not reduced to very small duty cycles, pulse skipping does not occur, and the associated voltage jitter does not happen.

An important design consideration for the current doubler topology is that the DC resistance of both halves must be equal. PCB layout must be as symmetrical as possible, and the DCRs of the inductors should be reasonably equal. If not, the current between the two sides does not split equally. Because perfect physical PCB symmetry is not always possible, current sharing between inductors must be confirmed.

In Figure 14, inductor current waveforms are taken from the ISL6752/54EVAL1Z board. Current balance between the two inductors was achieved after one board revision. The inductor currents maintain the same waveform shape even at no load.

Another design consideration when using SRs is how to connect the outputs of multiple power supplies in parallel for redundancy or increased power capacity. A consequence of negative current flow in an SR (when a diode would otherwise be reverse biased and off) is that power can be transferred from the secondary to the primary if one of the paralleled outputs has a higher voltage. The voltage loop of the units with lower set point voltages attempts to pull down the voltage by sinking current from the higher set point units. The primary side bridge capacitor is charged by the secondary side, eventually resulting in excessive voltage damage. This damage can be avoided by using OR-ing diodes (or FETs) on the paralleled outputs. Another solution is to turn off the SRs (diode emulation mode) when the current reverses in the SRs, but this eliminates some of the advantages of using SRs. Paralleling features are not implemented on the ISL6752/54EVAL1Z board.
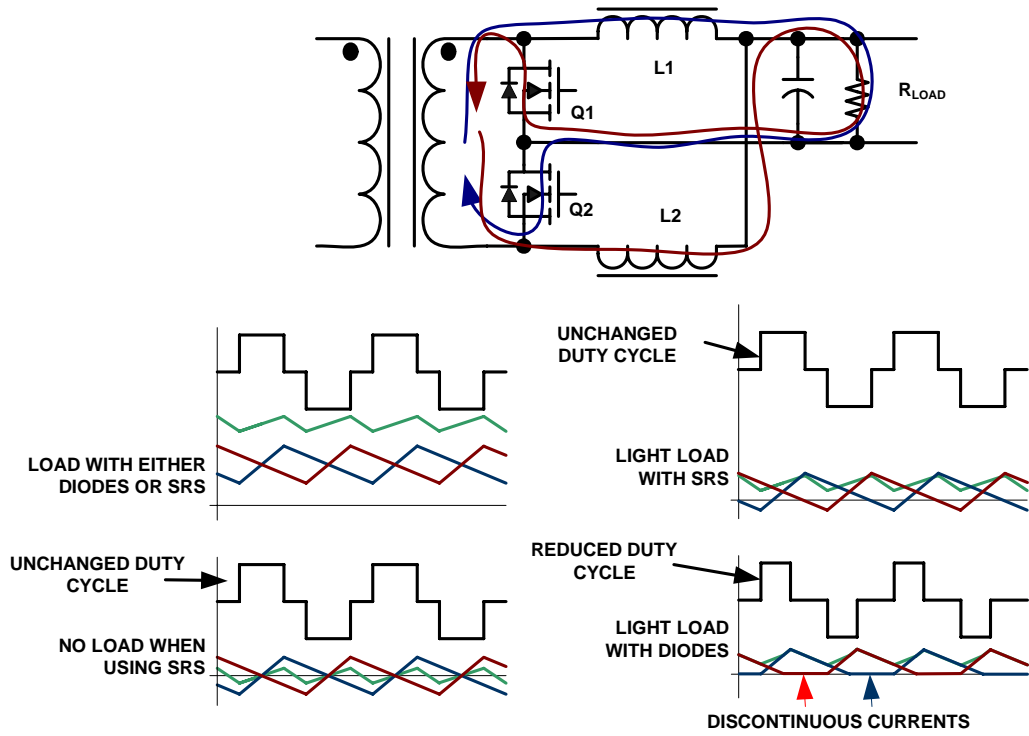
FIGURE 13. CURRENT FLOW IN TWO INDUCTORS OF CURRENT DOUBLER TOPOLOGY

In the diagram labels:
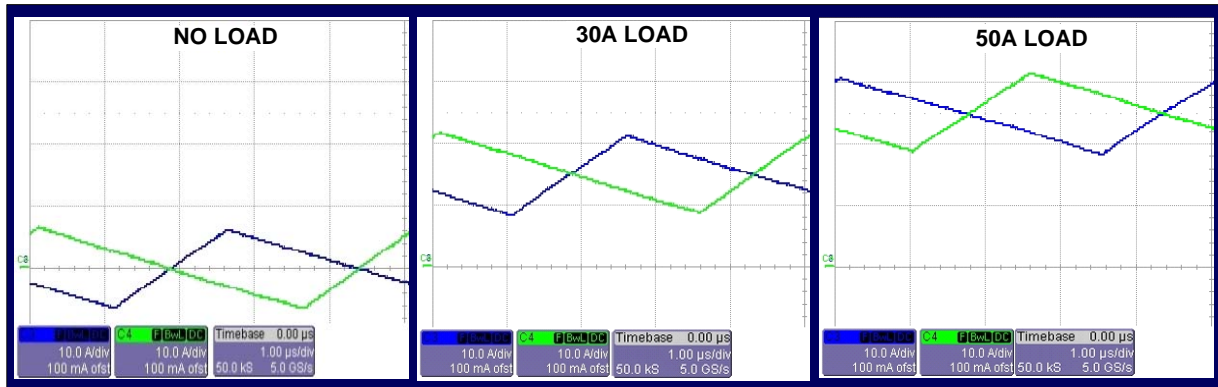- L1
- Q1
- L2
- Q2
- R$_{LOAD}$

UNCHANGED DUTY CYCLE

LOAD WITH EITHER DIODES OR SRS

LIGHT LOAD WITH SRS

UNCHANGED DUTY CYCLE

NO LOAD WHEN USING SRS

REDUCED DUTY CYCLE

LIGHT LOAD WITH DIODES

DISCONTINUOUS CURRENTS



FIGURE 14. INDUCTOR CURRENT WAVEFORMS

NO LOAD

30A LOAD

50A LOAD

# Current Sensing

Current flowing from the secondary to the primary can result in an unanticipated malfunction of the current sensing transformer circuit if reverse SR currents are not considered. Figure 15 shows a commonly used primary side current sensing circuit utilizing one current sensing transformer (CT).
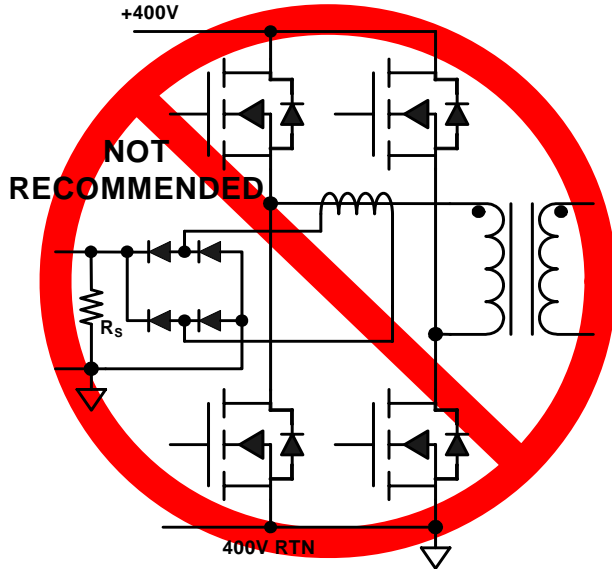


FIGURE 15.  PRIMARY SIDE CURRENT SENSING CIRCUIT UTILIZING ONE CT

This circuit works well for peak current mode control if power is always flowing from primary to secondary, as is the case when diodes are used instead of SRs. Figure 16 illustrates the performance of the current sensing output when power always flows from primary to secondary.
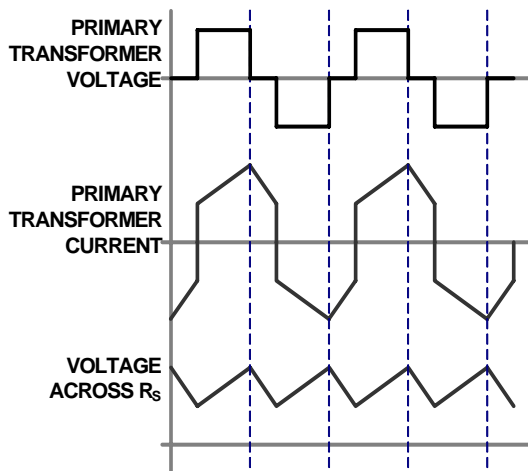


FIGURE 16.  PERFORMANCE OF CURRENT SENSING OUTPUT

The voltage across $R_S$ is as expected. The vertical dashed lines show when the power cycle is terminated at the required peak of the current.

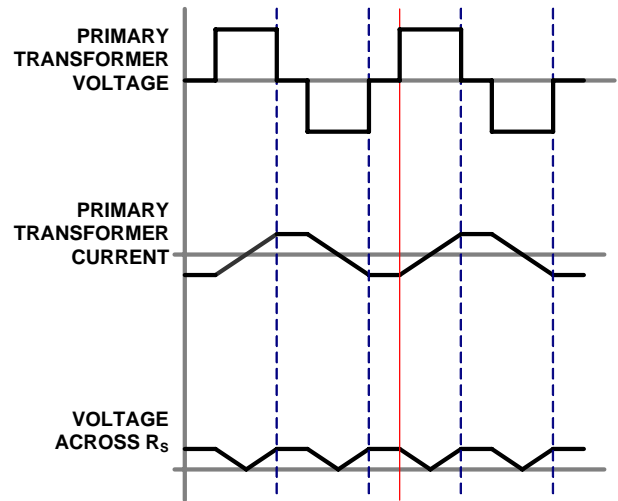Figure 17 illustrates what happens at no load to the sense voltage across $R_S$.



FIGURE 17.  NO LOAD SENSE VOLTAGE ACROSS $R_S$

Notice that the negative components of the primary transformer current are rectified, resulting in two peaks of current across $R_S$ for each half cycle. Under steady state conditions, the rectified negative component may cause erratic performance because the cycle can terminate on the first peak (the inverted peak, as indicated by the vertical red line) instead of the required second peak. This condition can easily be corrected by having a small load across the output to ensure that the negative peak is always less than the positive.

A minimum load, however, does not correct a more serious problem that occurs when there is a large load step from a heavy load to no load. When the load current is interrupted, the output capacitor charges higher than the regulated voltage. As the regulation loop is starting to respond by slewing to a minimum duty cycle, the excessive voltage on the output capacitor starts to discharge back to the primary. This results in a large negative current at the beginning of the duty cycle, which causes the duty cycle to be terminated very early. The imbalance of the applied volt-seconds to the power transformer may saturate the power transformer and damage the power bridge.

Another scenario is that the current sensing transformer itself may saturate, which also damages the bridge. The control loop cannot maintain balanced alternate half cycles applied to the power transformer without valid current sense information.

There are three solutions to this problem. Figure 18 illustrates the placements of two current sensing transformers, one on each drain leg of the bottom FETs.

In this configuration, only positive current flowing into the drains of the bottom FETs are sensed across $R_S$, solving the problem of rectified negative currents being impressed across $R_S$. An advantage of using two CTs is that there is a full half cycle available to reset the cores of the CTs. This is the solution used in the ISL6752/54EVAL1Z board.
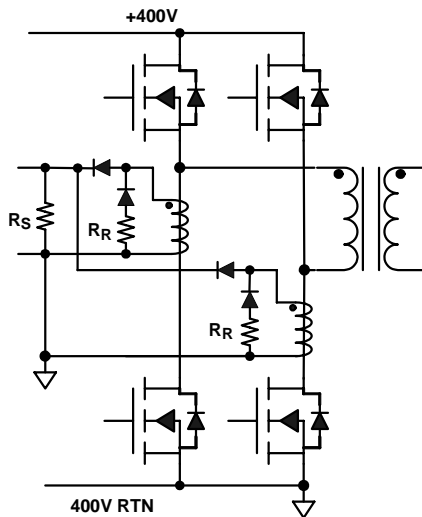
**FIGURE 18. PLACEMENT OF TWO CURRENT SENSING TRANSFORMERS**

Figure 19 shows a different current sensing implementation that also solves the problem shown in Figure 15. In this example, both drain currents of the bottom FETs are sensed by only one CT. There are some limitations that must be considered, however. The minimum time available to reset the core is the duration of the selected dead time between the two FETs on the same side of the bridge. To accommodate the resetting of the CT, this dead time can be made longer, but the consequences of reducing the maximum duty cycle available for output voltage regulation must be considered.
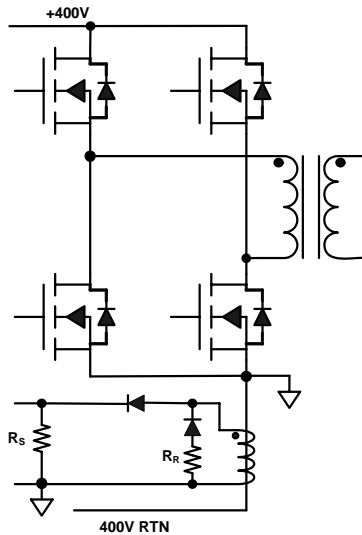


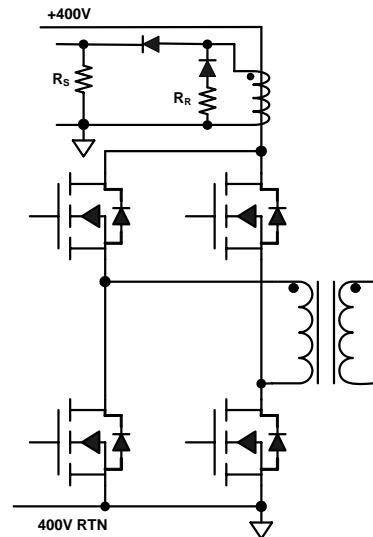**FIGURE 19. CURRENT SENSING TRANSFORMER IN THE COMMON SOURCE LEAD**

If the dead time is kept short, then the peak voltage required for resetting the core is relatively large. For example, assume that the selected dead time is 2% of the duty cycle. The resulting worst-case reset voltage is shown approximately in Equation 1:

$$(0.98 / 0.02) \cdot V_{SMAX} = 49V \qquad \text{(EQ. 1)}$$

In Equation 1, $V_{SMAX}$ is 1V (the current limit voltage of the ISL6752); this is the ideal reset voltage. In practice, however, the parasitic capacitance of the output windings suppresses the peak voltage, and consequently, the reset time increases. If a custom current sensing transformer is designed, the effects of the parasitic capacitance can be minimized by increasing the space between turns. If a standard, off-the-shelf transformer is used, however, the output capacitance may be too large to allow long duty cycles. In this case, the two-transformer solution may be necessary.

Notice in Figure 19 that the 400V RTN is slightly more negative than signal ground. This configuration is recommended for applications that directly drive the bottom FETs with MOSFET drivers. If the 400V RTN and the MOSFET drivers are grounded, regenerative feedback will be present on the output of the MOSFET drivers because of the CT windings in the gate drive loop.

A variation on the current sense circuit in Figure 19 is to place the current sensing transformer in the common drain lead of the two high-side FETs, as shown in Figure 20.



**FIGURE 20. CURRENT SENSING TRANSFORMER IN THE COMMON DRAIN LEAD**

The circuits shown in Figures 19 and 20 give exactly the same performance, but the problem associated with the gate drives (as explained in Figure 19) is avoided. The disadvantage of placing the CT at this location is that the CT must be designed with 400VDC operational insulation.

# Conclusion

This application note reviews the use of MOSFETs as synchronous rectifiers to replace conventional diodes. The advantages of improved power efficiency and load transient are reviewed along with implementation problems that must be solved.

The use of daughter cards for the ISL6752 and ISL6754 control ICs also allows comparison of cycle-by-cycle peak current limiting and average current limiting.

# References

[1] Fred Greenfeld, Intersil Application Note AN1246, "Techniques to Improve ZVS Full-bridge Performance"

[2] Fred Greenfeld, Intersil Application Note AN1262, "Designing with the ISL6752, ISL6753 ZVS Full-bridge Controllers"

[3] Richard Garcia, Intersil Application Note AN1619, "Designing with ISL6752DBEVAL1Z and ISL6754DBEVAL1Z Control Cards"

# Evaluation Board Set-up

The following sections cover the set-up of the ISL6752/54EVAL1Z evaluation board. Also included are waveforms, performance parameters, PCB layout, and schematics.

# Setting Up

### Danger

- This evaluation unit should be used and operated only by persons experienced and knowledgeable in the design and operation of high voltage power conversion equipment.

- Use of this evaluation unit constitutes acceptance of all risk inherent in the operation of equipment having accessible hazardous voltage. Careless operation may result in serious injury or death.

- Use safety glasses or other suitable eye protection.

- A line isolated 400VDC supply is required.

### Lab Equipment Required

- DC bias power supply, 12.6VDC @ 200mA minimum

- Adjustable 0VDC-400VDC regulated lab power supply, 2.5ADC minimum with current limit

- Fan to cool heatsinks

- Oscilloscope, digital preferred, with 4 channels, 20MHz minimum bandwidth

- Adjustable DC load (electronic or resistor), 70A @ 12V, 100A @ 0V min, >850W

- DC Multimeter

- Infra-red temperature probe (optional but highly recommended)

### Turn-On Procedure

1. Solder a wire between DISABLE and PGND-1 lugs located on the lower left side of the main board. Optionally connect a switch between these two lugs.

2. Install either of the daughter control cards onto the main board.

3. Connect the DC load to the outputs of the evaluation board. Adjust the load to zero current.

4. With both supplies turned off, connect the DC bias supply to the +13V terminal and PGND.

5. Connect the 400V supply to +400V and 400V RTN.

6. Turn on the DC bias supply and adjust the current limit to 200mA. Adjust the voltage to +12.6 VDC. The lab supply current should be approximately 150mA.

### Caution

A voltage clamp, D3, is used to protect the primary side control circuit from catastrophic damage should the high voltage bridge fail. In order to prevent this clamp from conducting, do not adjust the bias supply above 13.5VDC.

7. Turn on the 400V supply and adjust the current limit to 2.5A. Adjust the voltage to 400VDC. *Do not exceed 450VDC.* The current should be approximately 45mA.

8. Turn on the fan and direct the air flow through the heatsinks mounted on the bottom of the board.

9. Using the test points that are adjacent to the output power lugs, measure the output voltage of 12V ±0.5VDC.

The output load and input voltage can now be safely adjusted.

Because there is no thermal shut-down circuit, it is important to maintain adequate airflow over the heatsinks, especially when applying large loads. It is recommended to measure the temperature of the power FETs (primary bridge and secondary SRs) to ensure that their temperatures do not exceed +85°C. It is usually necessary to have only a moderate airflow over the heatsinks, even under worst-case loads.

# Waveforms

## ZVS

In Figure 21, the drain-source voltage of the low-side FETs relative to the gate voltage is displayed to highlight the ZVS performance of the bridge. The load is at the rated 50A. Notice that full ZVS is not achieved because the minimum resonance voltage is about 25VDC. Also, the gate drive is turning on late (about 25ns), allowing the resonant voltage to start rising. Even though the optimum zero voltage switching is not achieved, 98% of the switching losses are still recovered [$(400^2$-$50^2)$/ $400^2$ = 98%]. This improvement over the ISL6752EVALZ was achieved by increasing the leakage inductance of the transformer and by using bridge FETs with less body capacitance.

In Figure 22, resonant switching with 50% load still saves 84% of the switching losses. Other techniques can be used to improve ZVS performance. For more information, see Application Note AN1246, "Techniques to Improve ZVS Ful-bridge Performance".

## ZVS Waveforms
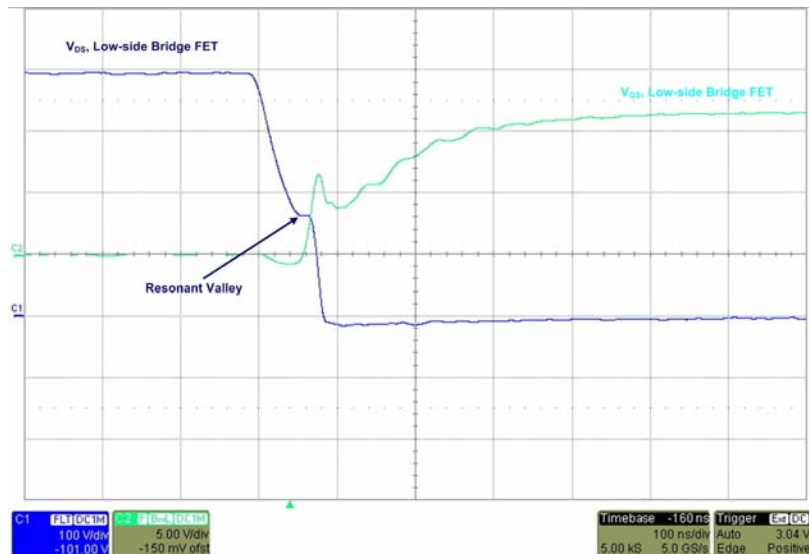


**FIGURE 21.  RESONANT SWITCHING WITH 100% (50A) LOAD**



**FIGURE 22.  RESONANT SWITCHING WITH 50% (25A) LOAD**
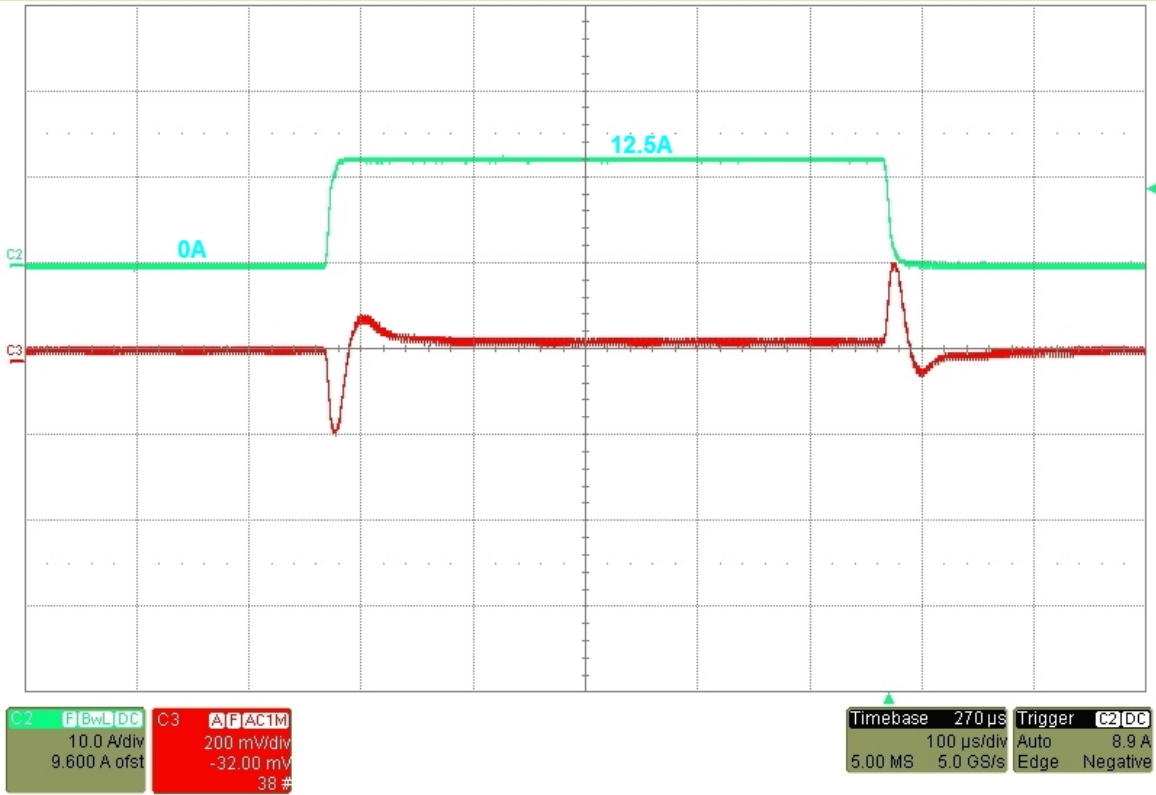
## Load Transients Waveforms



**FIGURE 23.  STEP LOAD: 0A TO 12.5A (12.5A DELTA)**



**FIGURE 24.  STEP LOAD: 25A TO 37.5A (12.5A DELTA)**

## Load Transients Waveforms (Continued)



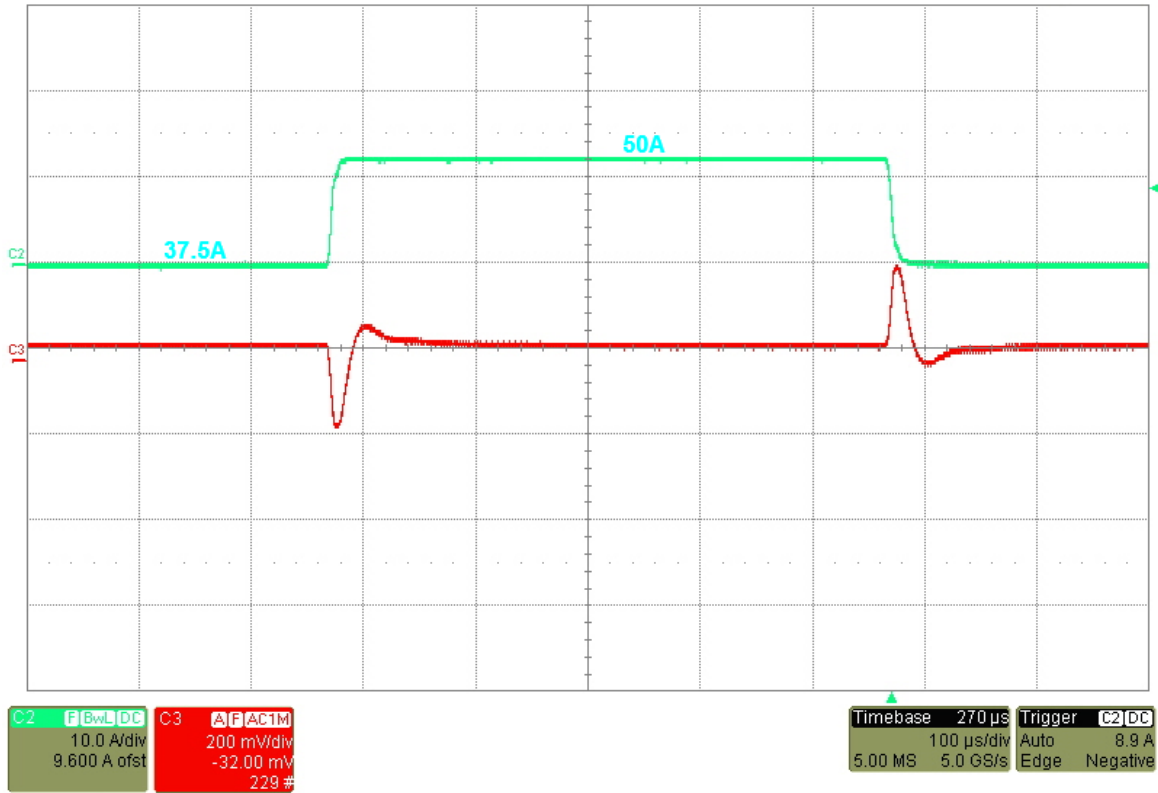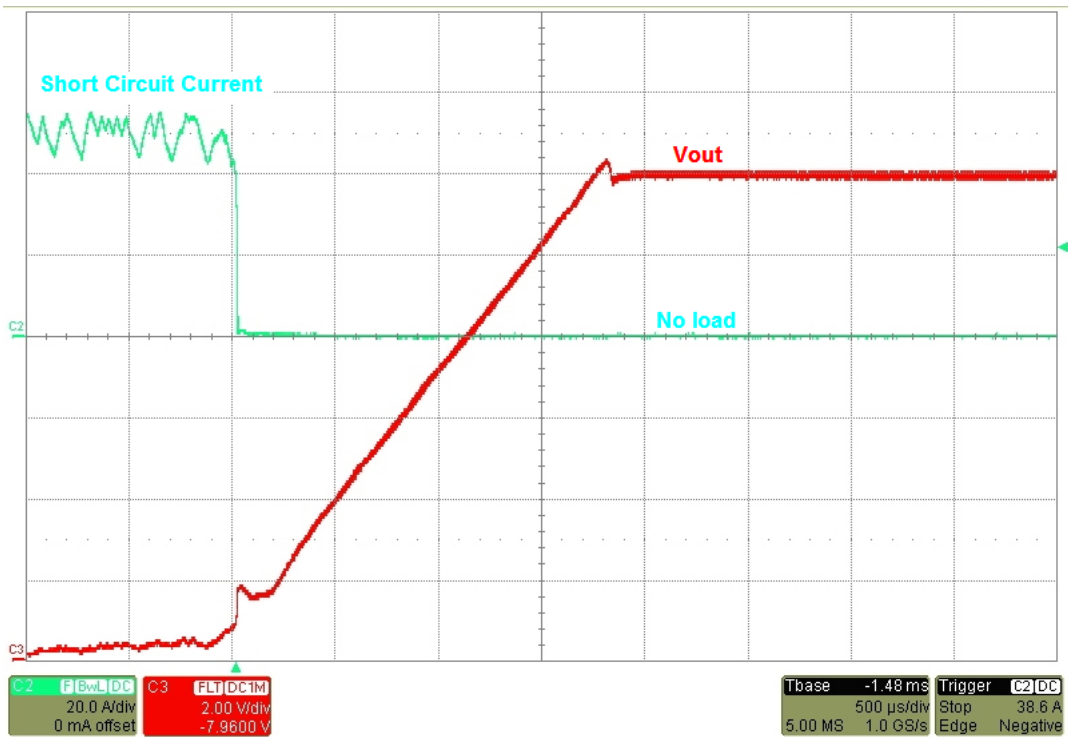**FIGURE 25. STEP LOAD: 37.5A TO 50A**



**FIGURE 26. STEP LOAD: 0A TO 25A**

## Load Transients Waveforms (Continued)



**FIGURE 27. STEP LOAD: 0A TO 50A**



**NOTE:**

$V_{OUT}$ recovers after a short circuit is removed when using the ISL6754DBEVAL controller.

After the short is removed, $V_{OUT}$ increases linearly because the output capacitance is being charged with a constant current (~55A).

**FIGURE 28. SHORT CIRCUIT RELEASE WITH ISL6754**

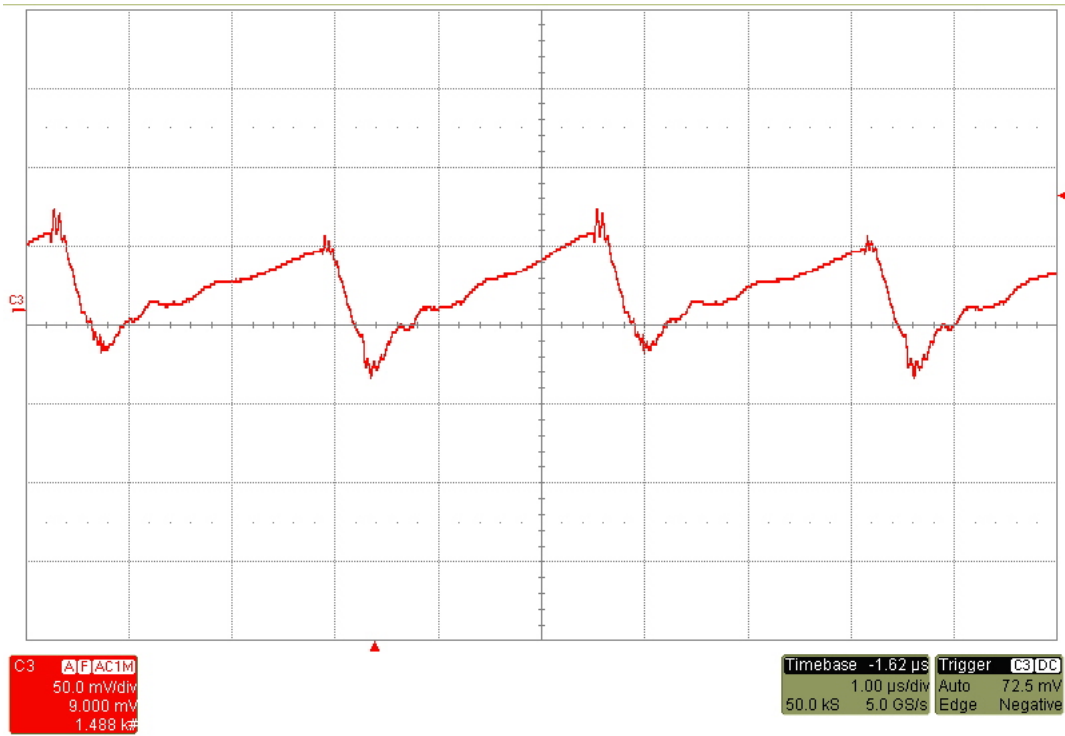intersil

## Output Ripple and Noise Waveforms



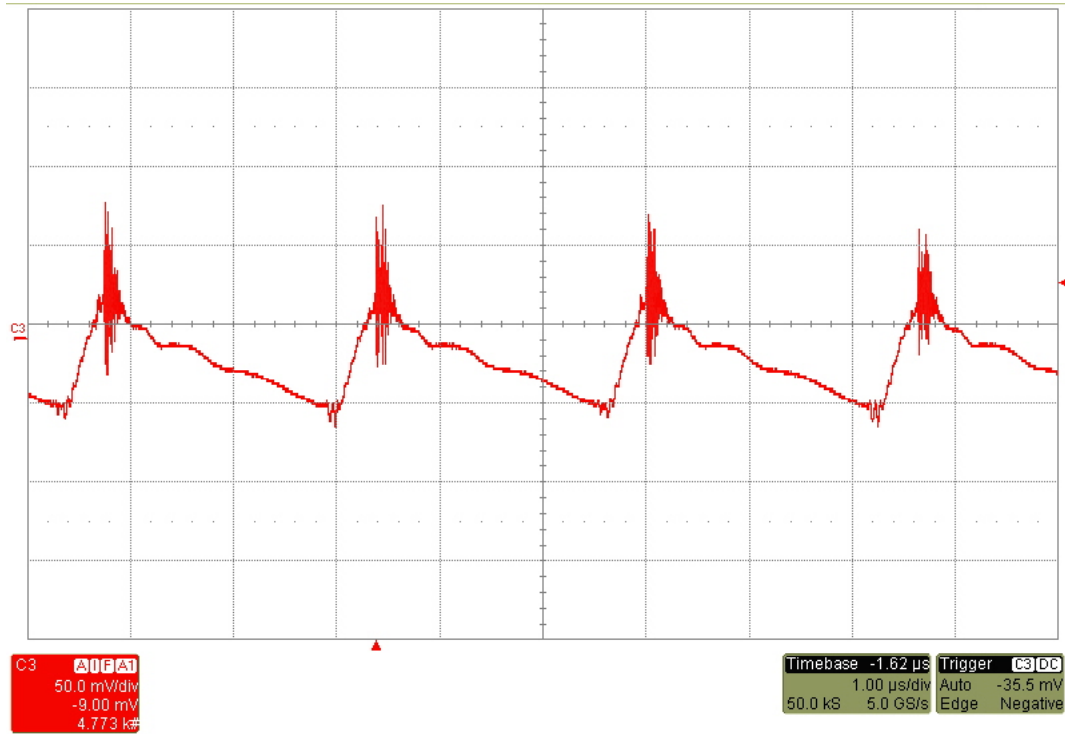**FIGURE 29.  OUTPUT RIPPLE, 50A LOAD, 40MHz BANDWIDTH**



**FIGURE 30.  OUTPUT RIPPLE, 50A LOAD, 145MHz BANDWIDTH**

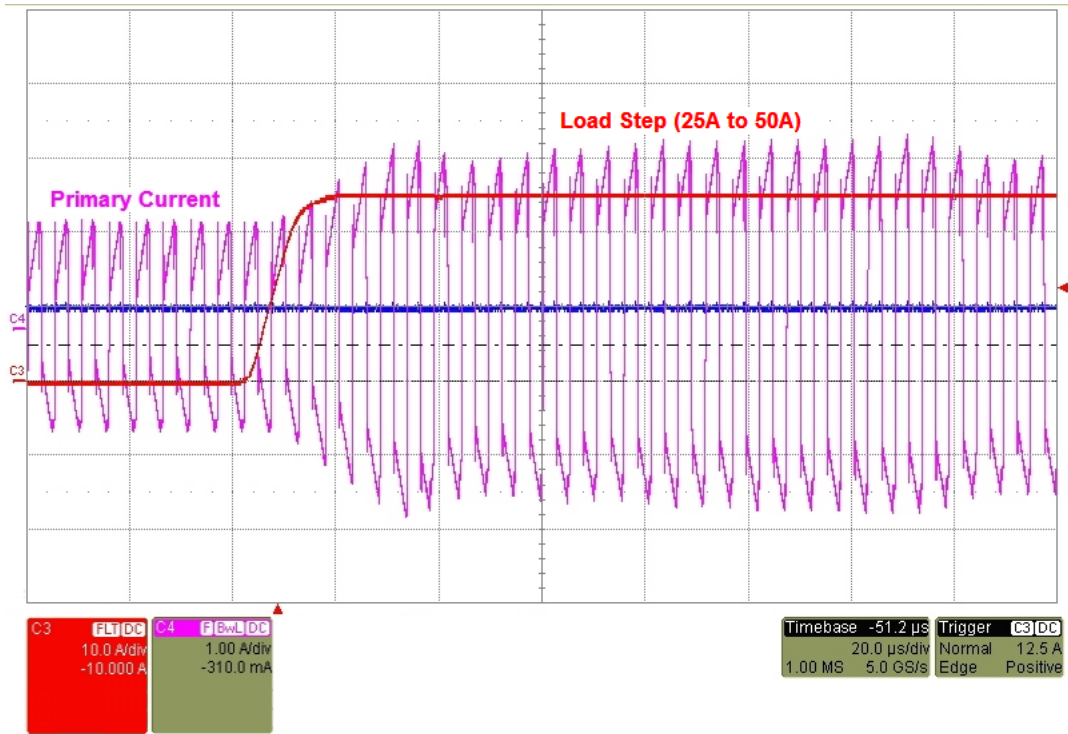## Transformer Current, Primary Winding Waveforms



**FIGURE 31. PRIMARY TRANSFORMER CURRENT vs OUTPUT LOAD TRANSIENT (25A TO 50A)**
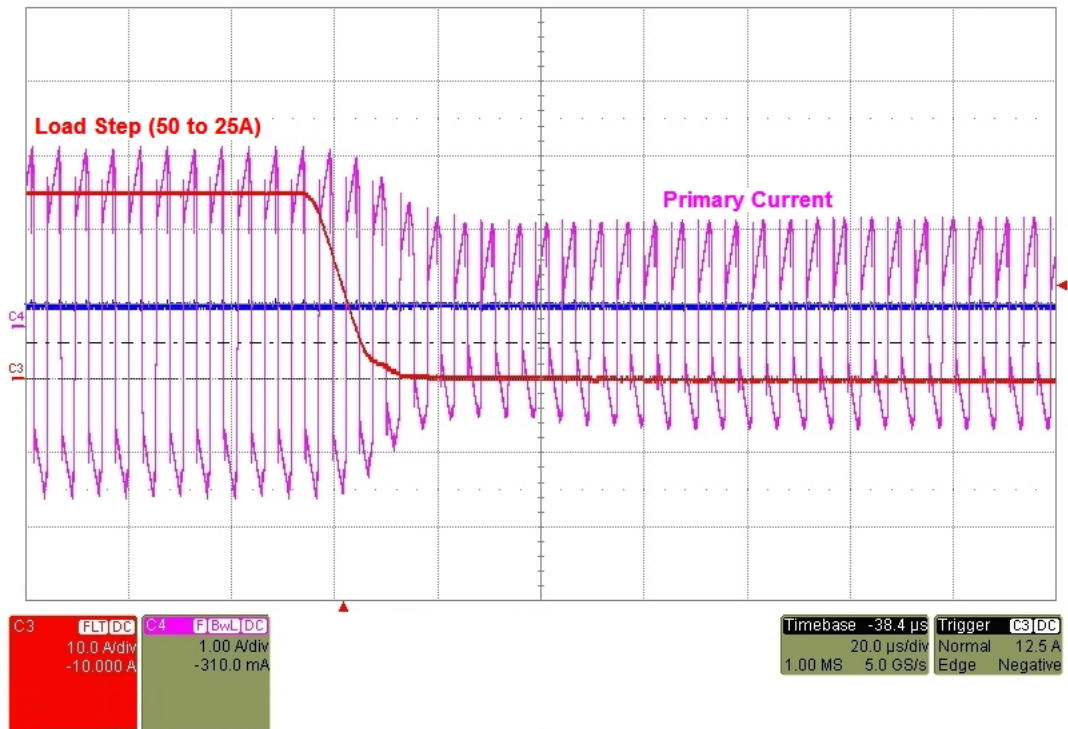


**FIGURE 32. PRIMARY TRANSFORMER CURRENT vs OUTPUT LOAD TRANSIENT (50A TO 25A)**
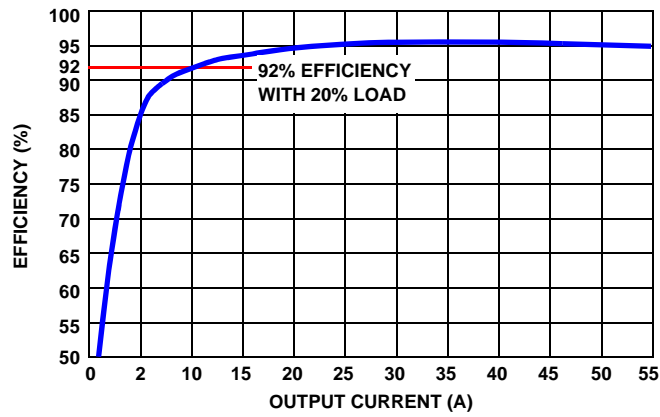
# Performance Curves



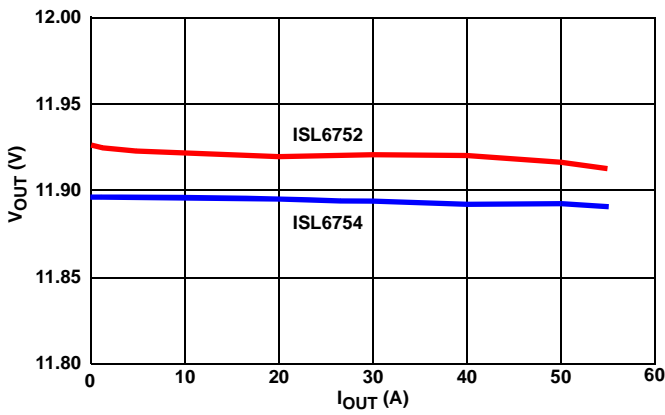**FIGURE 33. POWER EFFICIENCY vs LOAD (ISL6752 OR ISL6754)**
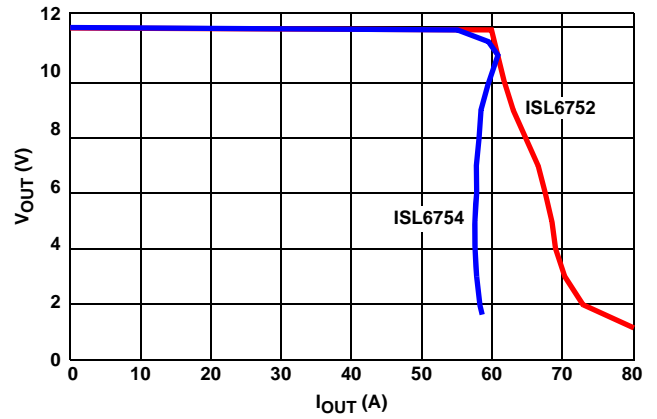


**FIGURE 34. LOAD REGULATION**



**FIGURE 35. PULSE BY PULSE vs AVERAGE CURRENT LIMIT**

# PCB Layout
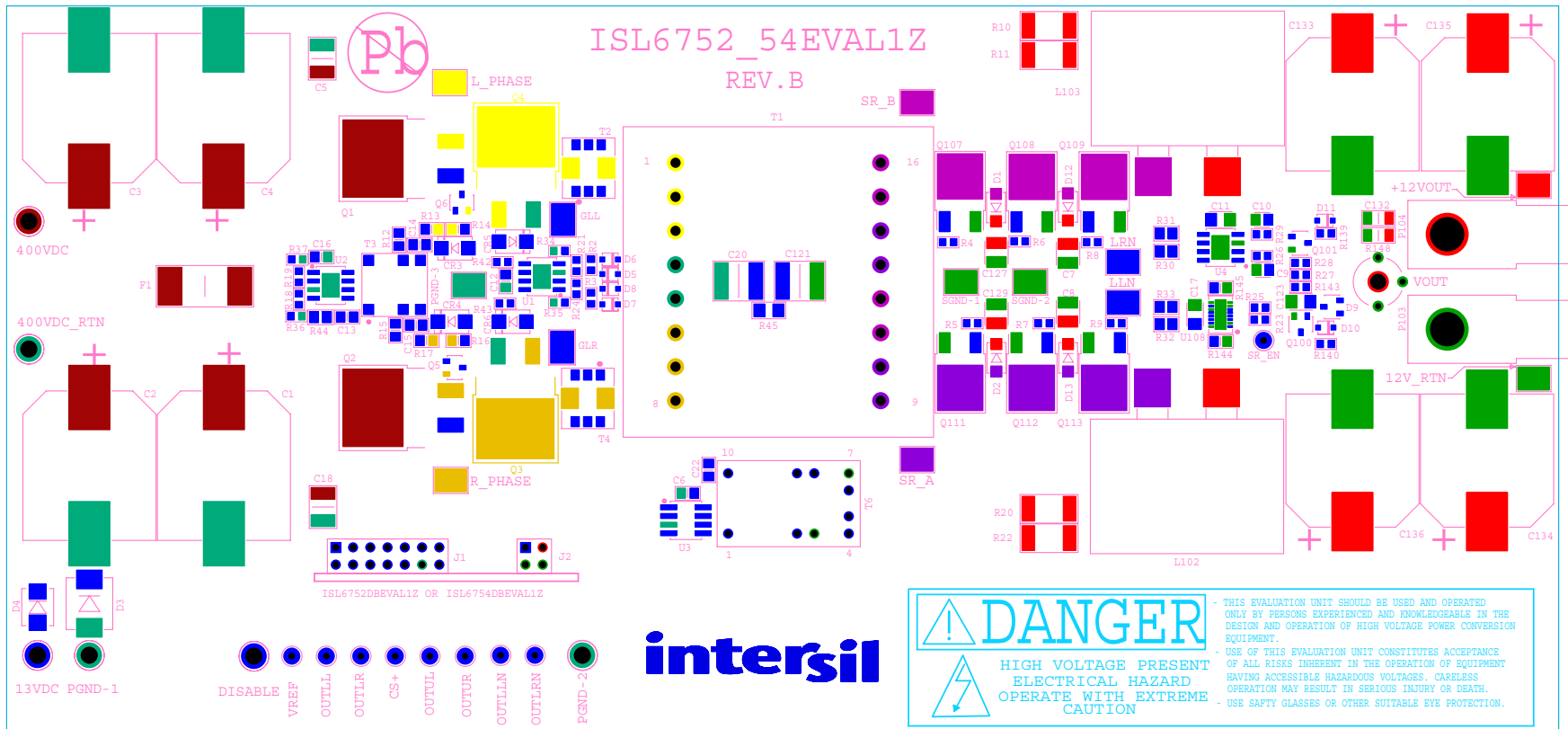
**FIGURE 36. SILKSCREEN TOP**

# PCB Layout (Continued)
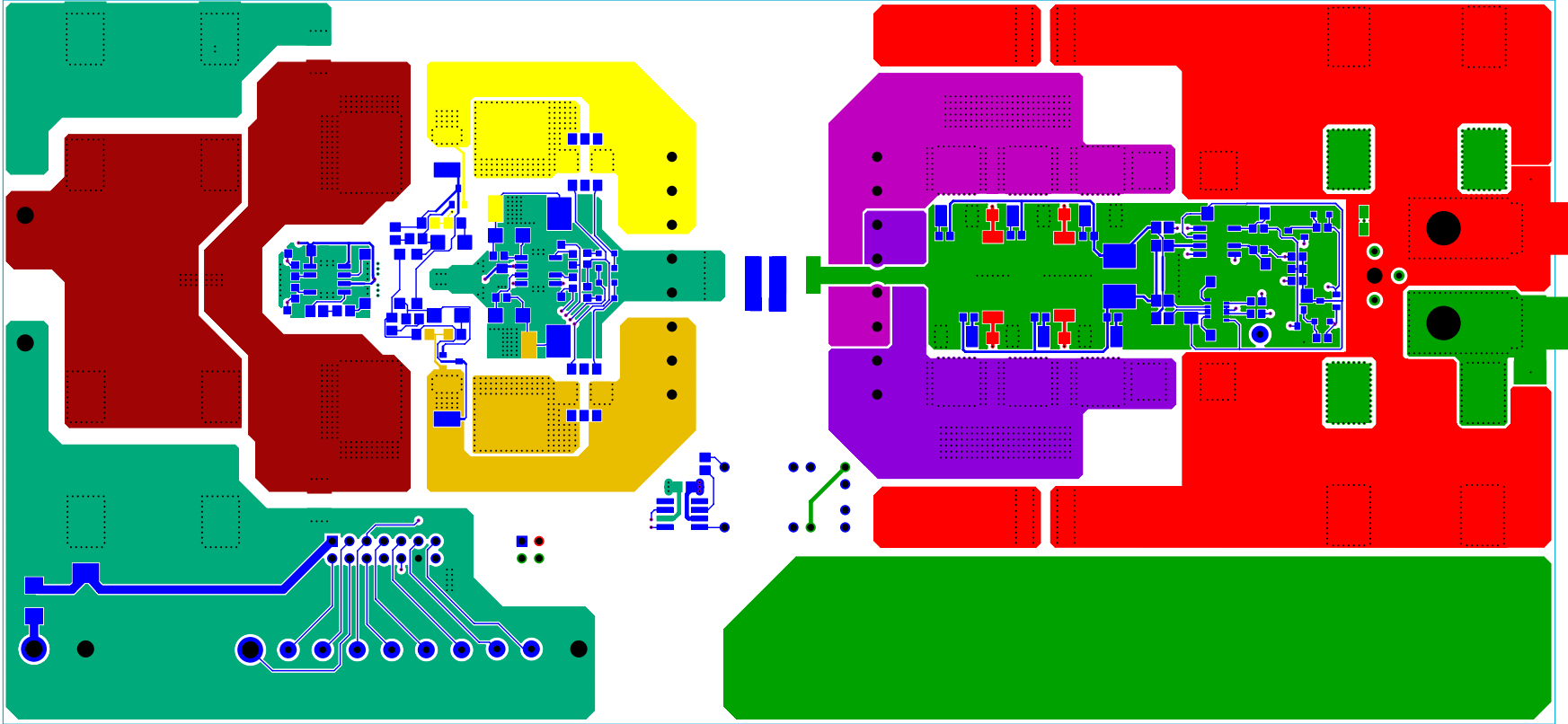
LAYER 1

**FIGURE 37. LAYER 1**
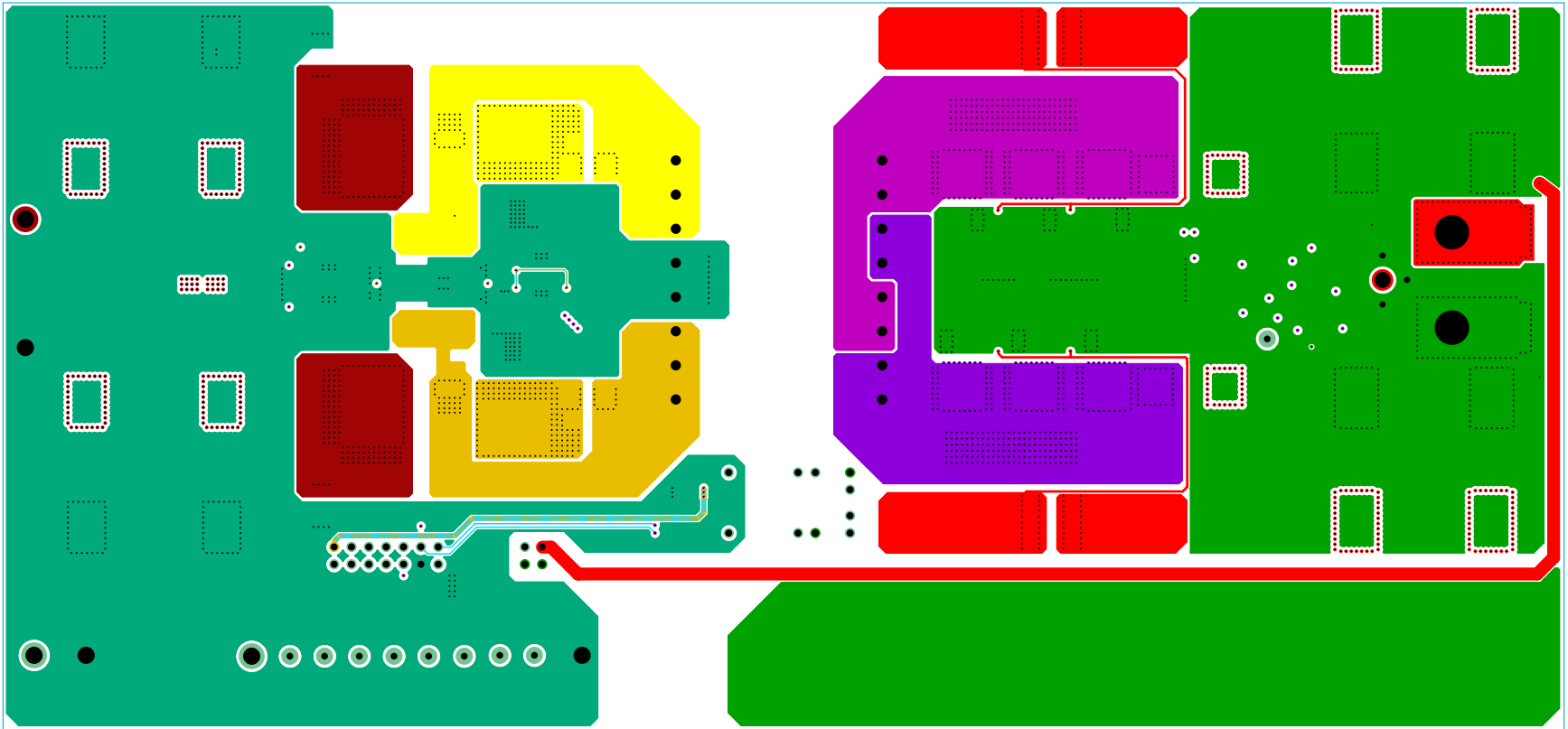
LAYER 2

**FIGURE 38. LAYER 2**
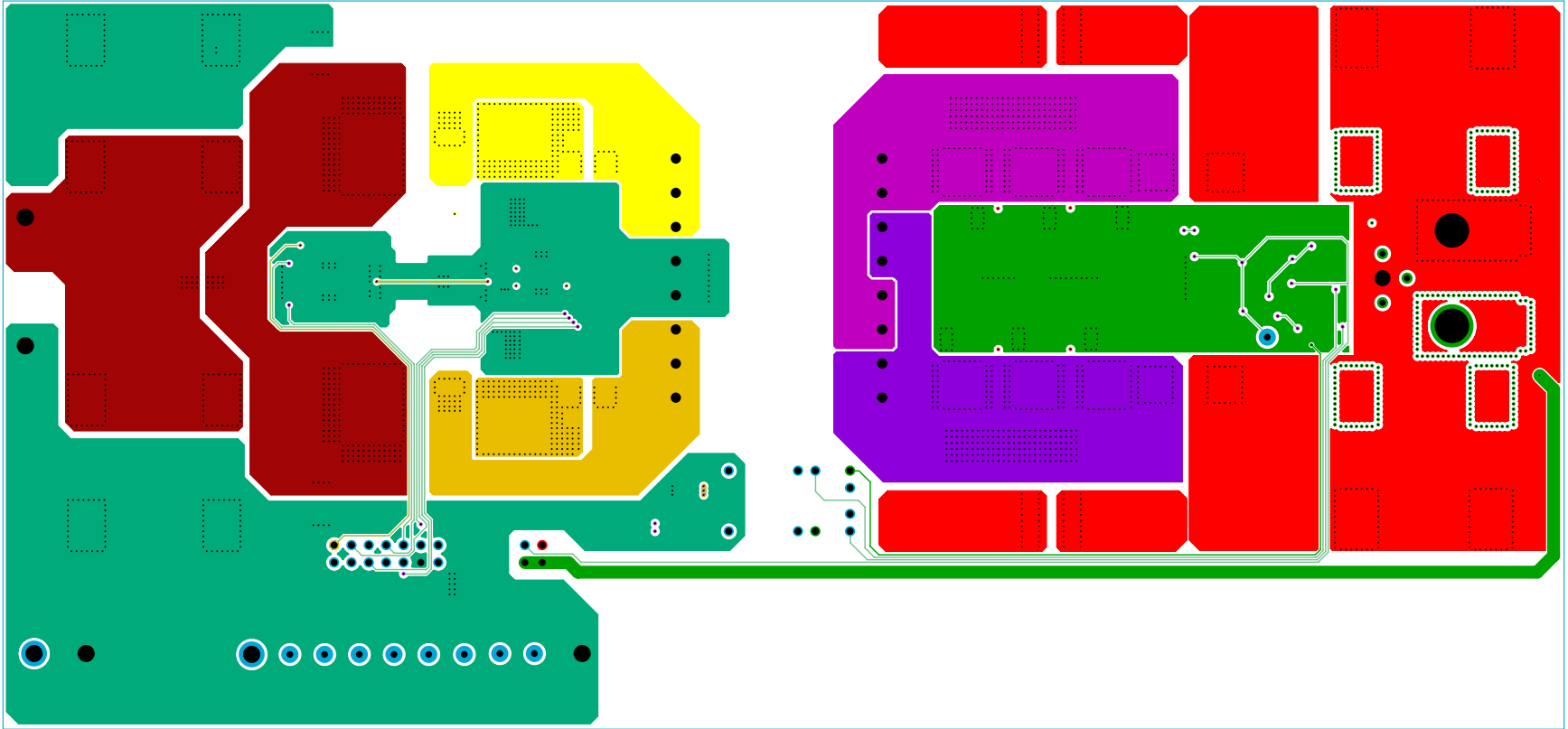
LAYER 3

**FIGURE 39. LAYER 3**

**Application Note 1603**
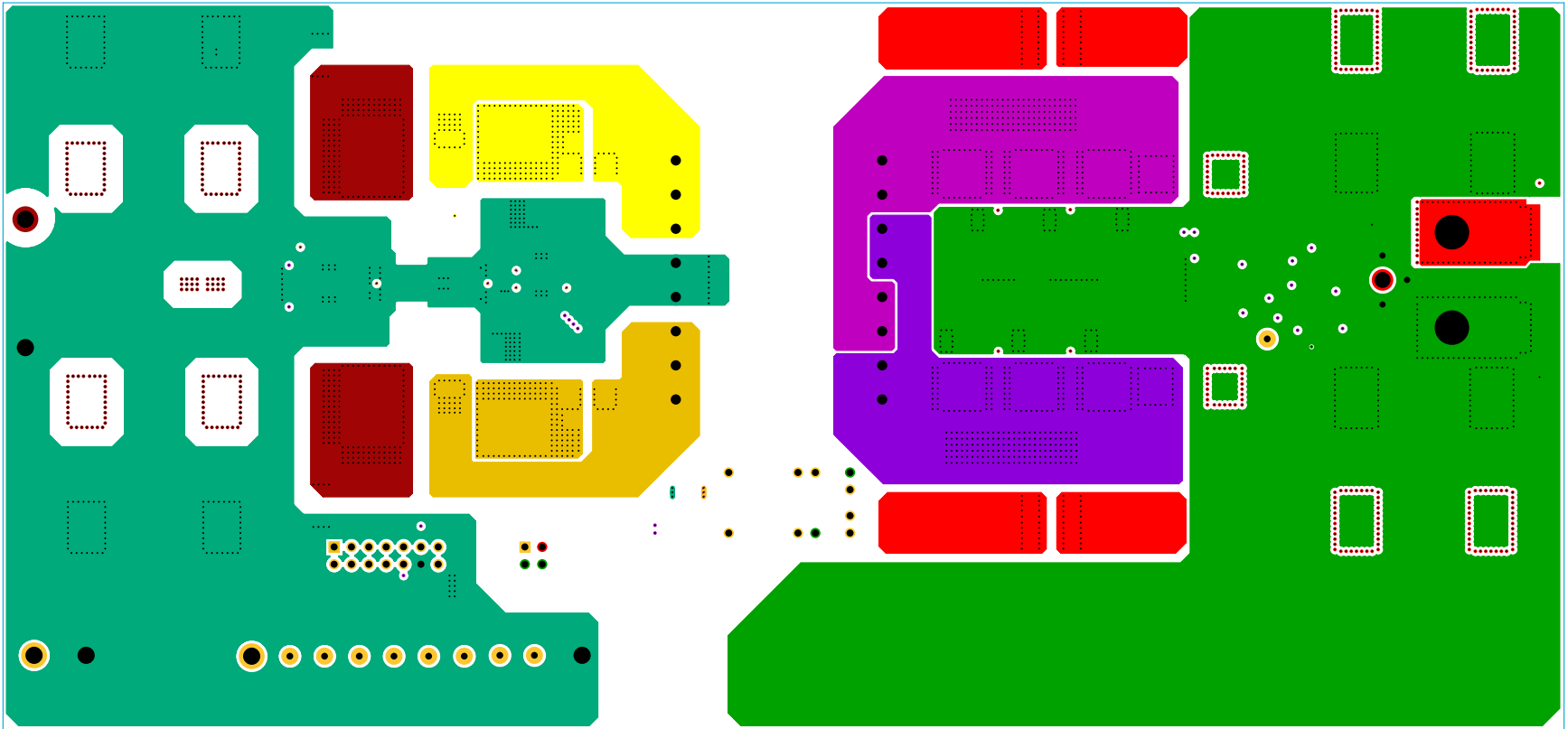
LAYER 4

**FIGURE 40.  LAYER 4**

Application Note 1603
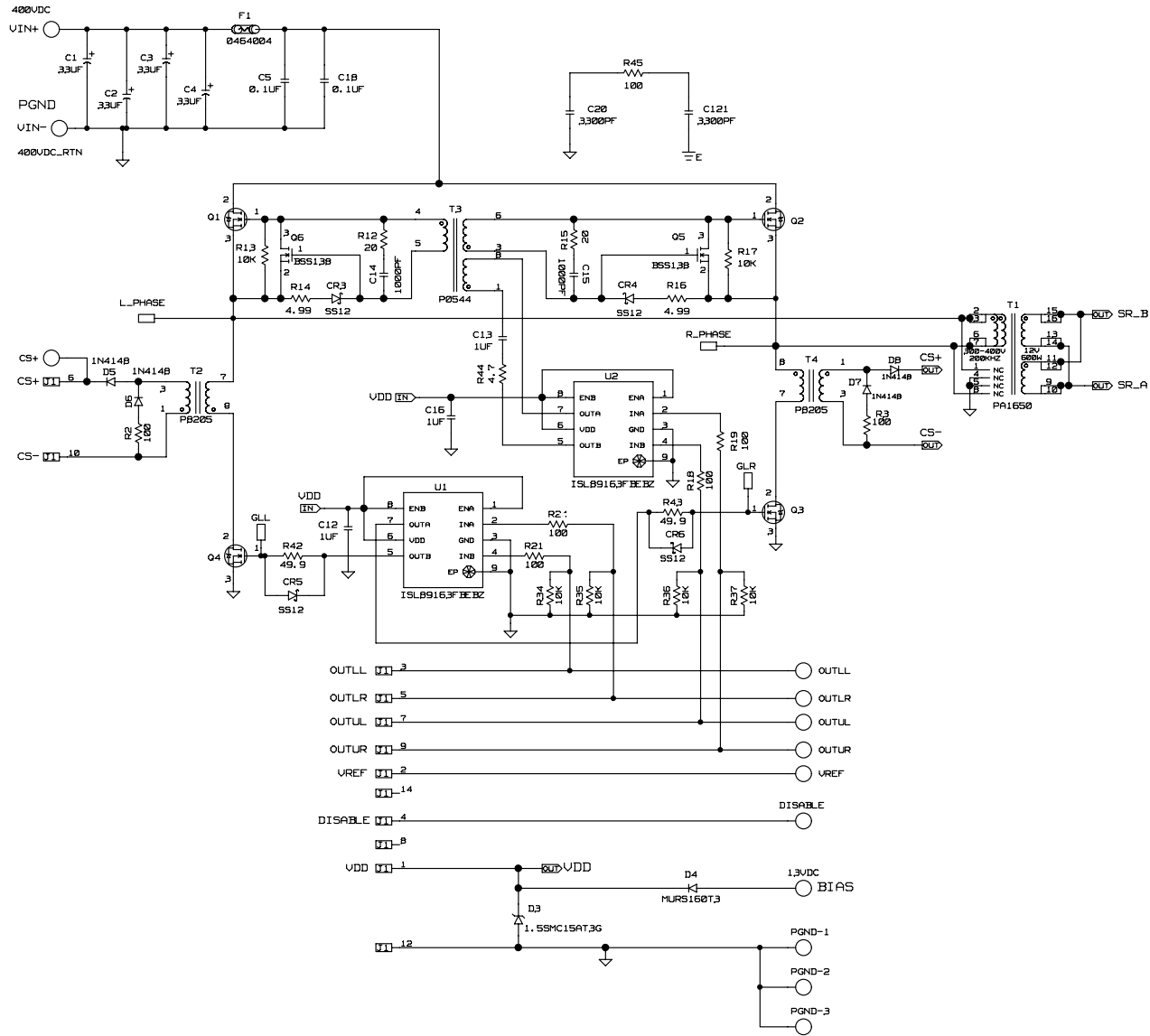
**FIGURE 41. MAIN BOARD, PRIMARY, ISL6752_54EVAL1Z**

Application Note 1603



FIGURE 42.  MAIN BOARD, SECONDARY, ISL6752_54EVAL1Z

# Schematics - Daughter Card
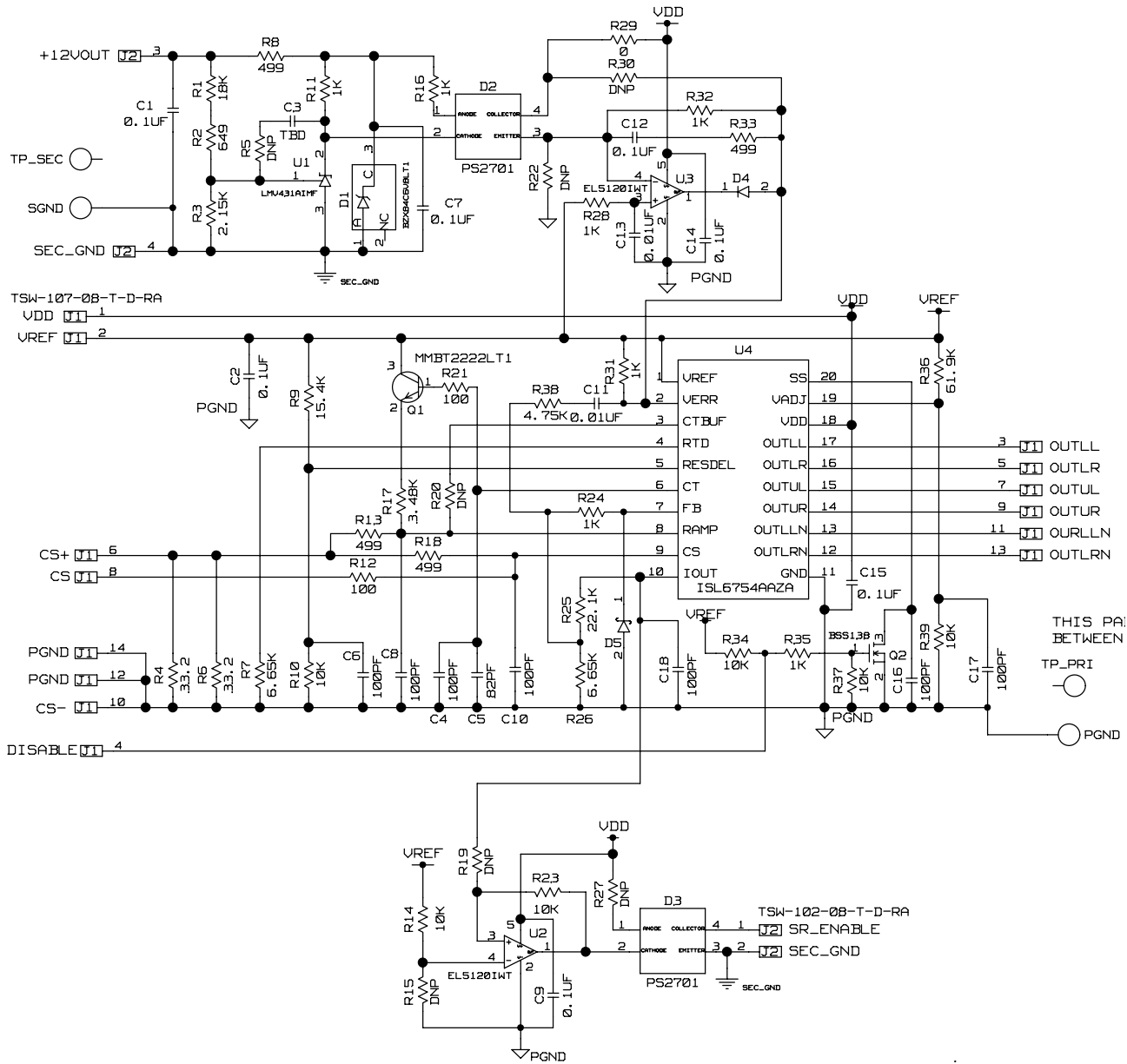
**FIGURE 43. DAUGHTER CARD, ISL6754DBEVAL**

**FIGURE 44. DAUGHTER CARD, ISL6752DBEVAL1Z**

# Bill of Materials

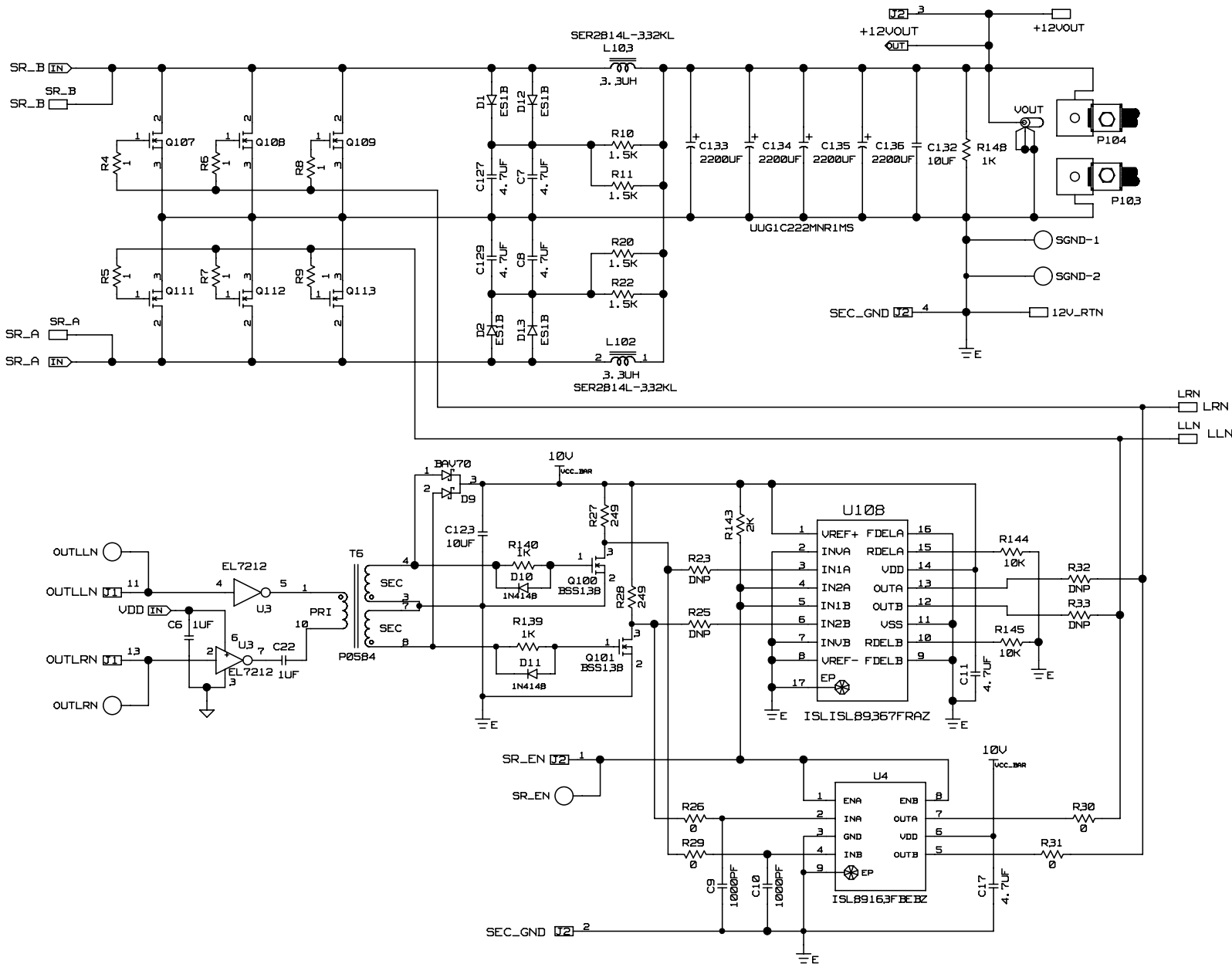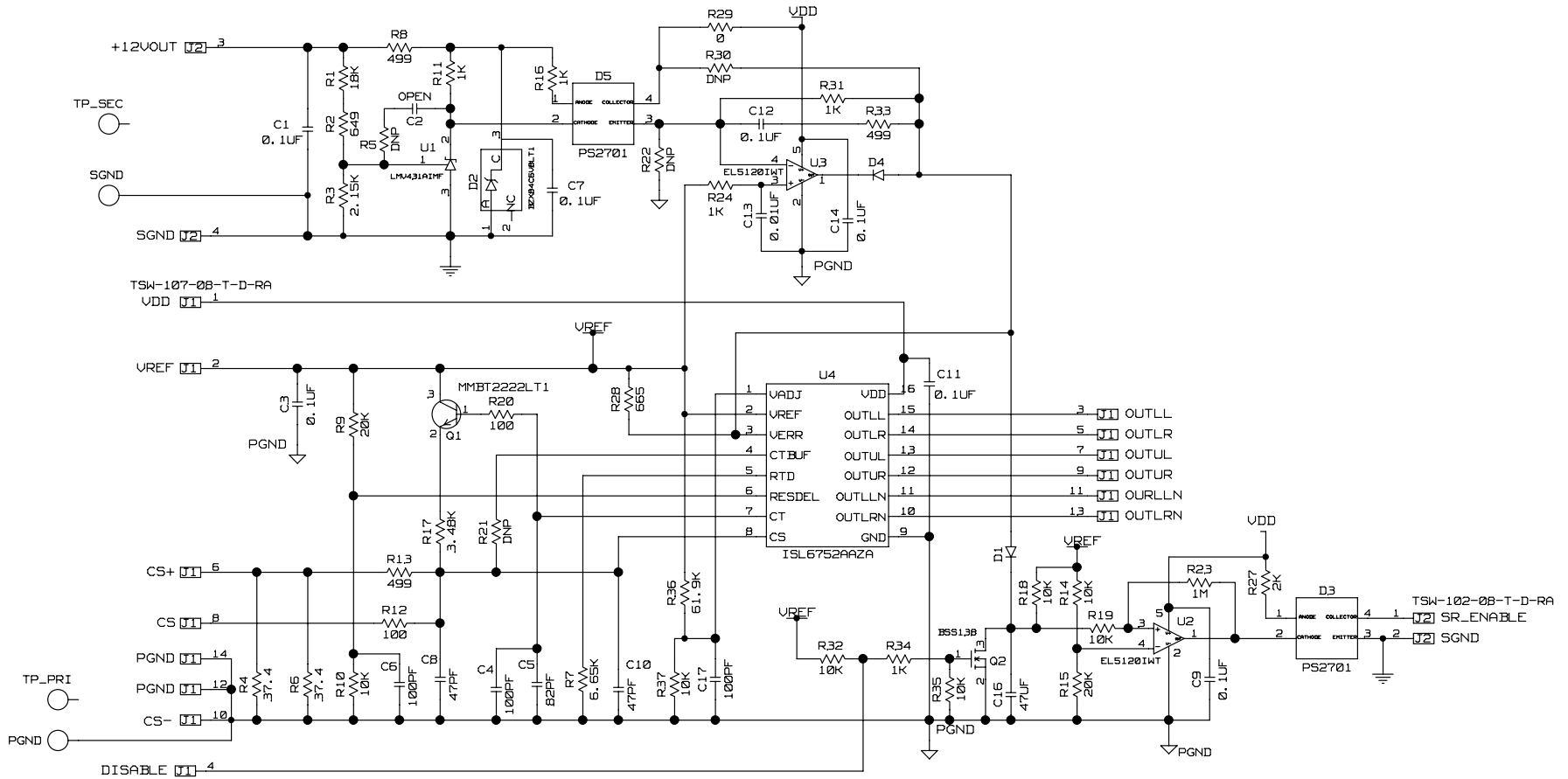| PART NUMBER | QTY | UNITS | REFERENCE DESIGNATOR | DESCRIPTION | MANUFACTURER | MANUFACTURER PART |
|---|---|---|---|---|---|---|
| ISL6752/54EVAL1ZREVBPCB | 1 | ea | | PWB-PCB, ISL6752_54EVAL1Z, REV B, ROHS | IMAGINEERING INC | ISL6752/54EVAL1ZREVBPC B |
| C3216X7R1C475K-T | 2 | ea | C11, C17 | CAPACITOR, SMD, 1206, 4.7µF, 16V, 10%, X7R, ROHS | TDK | C3216X7R1C475K |
| C4532X7R2J104K-T | 2 | ea | C5, C18 | CAP, SMD, 1812, 0.1µF, 630V, 10%, X7R, ROHS | TDK | C4532X7R2J104K |
| GA355QR7GF332KW01L-T | 2 | ea | C20, C121 | CAP, SMD, 2220, 3300pF, 250V, 10%, X7R, ROHS | MURATA | GA355QR7GF332KW01L |
| H1046-00102-100V10-T | 2 | ea | C14, C15 | CAP, SMD, 0805, 1000pF, 100V, 10%, X7R, ROHS | VENKEL | C0805X7R101-102KNE |
| H1046-00102-50V5-T | 2 | ea | C9, C10 | CAP, SMD, 0805, 1000pF, 50V, 5%, NP0, ROHS | PANASONIC | ECU-V1H102JCX |
| H1046-00105-25V10-T | 5 | ea | C6, C12, C13, C16, C22 | CAP, SMD, 0805, 1.0µF, 25V, 10%, X5R, ROHS | AVX | 08053C105KAT2A |
| H1065-00106-25V10-T | 1 | ea | C123, C132 | CAP, SMD, 1206, 10µF, 25V, 10%, X5R, ROHS | VENKEL | C1206X5R250-106KNE |
| H1082-00475-50V10-T | 4 | ea | C7, C8, C127, C129 | CAP, SMD, 1210, 4.7µF, 50V, 10%, X7R, ROHS | MURATA | GRM32ER71H475KA88L |
| SER2814L-332KL | 2 | ea | L102, L103 | COIL-PWR INDUCTOR, SMD, 3.3µH, 10%, 48A, 1.2mΩ, ROHS | COILCRAFT | SER2814L-332KL |
| UUG1C222MNL1ZD | 4 | ea | C133-C136 | CAP, SMD, 16X16.5, 2200µF, 16V, 20%, AL.EL., ROHS | NICHICON | UUG1C222MNL1ZD |
| UUG2W330MNL1MS | 4 | ea | C1-C4 | CAP, SMD, 18X21.5, 33µF, 450V, 20%, ALUM.ELEC, ROHS | NICHICON | UUG2W330MNL1MS |
| 131-4353-00 | 1 | ea | VOUT | CONN-SCOPE PROBE TEST PT, COMPACT, PCBMNT, ROHS | TEKTRONIX | 131-4353-00 |
| 1514-2 | 6 | ea | a) 13VDC, 400VDC, PGND-1, PGND-2, DISABLE | CONN-TURRET, TERMINAL POST, TH, ROHS | KEYSTONE | 1514-2 |
| 1514-2 | 0 | ea | b) 400VDC_RTN | CONN-TURRET, TERMINAL POST, TH, ROHS | KEYSTONE | 1514-2 |
| 5002 | 9 | ea | a) CS+, VREF, OUTLL, OUTLR, OUTUL, OUTUR | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS | KEYSTONE | 5002 |
| 5002 | 0 | ea | b) SR_EN, OUTLLN, OUTLRN | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS | KEYSTONE | 5002 |
| 5016-T | 13 | ea | a) GLL, GLR, LLN, LRN, SR_A, SR_B, PGND-3, 2, +12VOUT, 12V RTN | CONN-COMPACT TEST POINT, SMD, ROHS | KEYSTONE | 5016 |
| 5016-T | 0 | ea | b) SGND-1, SGND- | CONN-COMPACT TEST POINT, SMD, ROHS | KEYSTONE | 5016 |
| 5016-T | 0 | ea | c) L_PHASE, R_PHASE | CONN-COMPACT TEST POINT, SMD, ROHS | KEYSTONE | 5016 |

# Bill of Materials (Continued)

| PART NUMBER | QTY | UNITS | REFERENCE DESIGNATOR | DESCRIPTION | MANUFACTURER | MANUFACTURER PART |
|---|---|---|---|---|---|---|
| SLW-102-01-S-D | 1 | ea | J2 | CONN-SOCKET STRIP, LP, 2X2, 2.54mm, GOLD/TIN, ROHS | SAMTEC | SLW-102-01-S-D |
| SLW-107-01-S-D | 1 | ea | J1 | CONN-SOCKET STRIP, LP, 2X7, 2.54mm, GOLD/TIN, ROHS | SAMTEC | SLW-107-01-S-D |
| 1N4148WS-7-F-T | 6 | ea | D5-D8, D10, D11 | DIODE-RECTIFIER, SMD, SOD-323, 2P, 75V, 150mA, ROHS | DIODES INC. | 1N4148WS-7-F |
| BAV70-T | 1 | ea | D9 | DIODE-DUAL, SWITCHING, SMD, SOT23, 100V, 125mA, ROHS | NXP SEMICONDUCTORS | BAV70, 215 |
| ES1B-13-F-T | 4 | ea | D1, D2, D12, D13 | DIODE-RECTIFIER, SMD, 2P, SMA, 100V, 1A, ROHS | DIODES INC. | ES1B-13-F |
| MURS160T3G-T | 1 | ea | D4 | DIODE-RECTIFIER, SMD, SMB, 2P, 1A, 600V, ROHS | ON SEMICONDUCTOR | MURS160T3G |
| SS12T3G-T | 4 | ea | CR3-CR6 | DIODE-SCHOTTKY RECTIFIER, SMD, SMA, 2P, 20V, 1A, ROHS | ON SEMICONDUCTOR | SS12T3G (T3= T&R) |
| 0464004.DR | 1 | ea | F1 | FUSE, SMD, 12X4.5, 4A, 250V, NANO2 FAST ACTING, ROHS | LITTELFUSE | 0464004.DR |
| 1.5SMC15AT3G-T | 1 | ea | D3 | TVS, UNIDIRECTION, SMD, SMC, 1500W, 12.8V (peak rev) ROHS | ON SEMICONDUCTOR | 1.5SMC15AT3G |
| EL7212CSZ | 1 | ea | U3 | IC-DUAL CHANNEL MOSFET DRIVER, 8P, SOIC, ROHS | INTERSIL | EL7212CSZ |
| ISL89163FBEBZ | 3 | ea | U1, U2, U4 | IC-6A PWR MOSFET DRIVER, 8P, EPSOIC, ROHS | INTERSIL | ISL89163FBEBZ |
| ISL89367FRTAZ | 1 | ea | U108 | IC-6A MOSFET DRIVER, 12V INPUT, 16P, DFN, 3X5, ROHS | INTERSIL | ISL89367FRTAZ |
| BSS138LT1G-T | 4 | ea | Q5, Q6, Q100, Q101 | TRANSIST-MOS, N-CHANNEL, SMD, 3P, SOT23, 50V, 200mA, ROHS | ON SEMICONDUCTOR | BSS138LT1G |
| FDD6670A | 6 | ea | Q107-Q109, Q111-Q113 | TRANSISTOR-MOS, N-CHANNEL, SMD, DPAK, 30V, 66A, ROHS | FAIRCHILD | FDD6670A |
| SPB04N60C3 | 4 | ea | Q1-Q4 | TRANSIST-MOS, N-CHANNEL, 3P, PG-TO263-8, 650V, 4.5A, ROHS | INFINEON TECHNOLOGY | SPB04N60C3 |
| H2511-00010-1/10W1-T | 6 | ea | R4-R9 | RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS | PANASONIC | ERJ-3RQF1R0V |
| H2511-00R00-1/10W-T | 2 | ea | R26, R29 | RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS | VENKEL | CR0603-10W-000T |
| H2511-01000-1/10W1-T | 6 | ea | R2, R3, R18, R19, R21, R24 | RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-1000FT |

# Bill of Materials (Continued)

| PART NUMBER | QTY | UNITS | REFERENCE DESIGNATOR | DESCRIPTION | MANUFACTURER | MANUFACTURER PART |
|---|---|---|---|---|---|---|
| H2511-01001-1/10W1-T | 2 | ea | R139, R140 | RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS | PANASONIC | ERJ-3EKF1001V |
| H2511-01002-1/10W1-T | 4 | ea | R34-R37 | RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS | KOA | RK73H1JT1002F |
| H2511-02001-1/10W1-T | 1 | ea | R143 | RES, SMD, 0603, 2k, 1/10W, 1%, TF, ROHS | KOA | RK73H1JTTD2001F |
| H2511-02490-1/10W1-T | 2 | ea | R27, R28 | RES, SMD, 0603, 249Ω, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-2490FT |
| H2511-049R9-1/10W1-T | 2 | ea | R42, R43 | RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS | VENKEL | CR0603-10W-49R9FT |
| H2511-DNP | 0 | ea | R23, R25 | RES, SMD, 0603, DNP PLACEHOLDER, ROHS | | |
| H2512-00200-1/8W1-T | 2 | ea | R12, R15 | RES, SMD, 0805, 20Ω, 1/8W, 1%, TF, ROHS | KOA | RK73H2AT20R0F |
| H2512-004R7-1/8W1-T | 1 | ea | R44 | RES, SMD, 0805, 4.7Ω, 1/8W, 1%, TF, ROHS | YAGEO | RC0805FR-074R7L |
| H2512-00R00-1/8W-T | 2 | ea | R30, R31 | R30, R31 RES, SMD, 0805, 0Ω, 1/8W, TF, ROHS | YAGEO | RC0805JR-070RL |
| H2512-01002-1/8W1-T | 4 | ea | R13, R17, R144, R145 | RES, SMD, 0805, 10k, 1/8W, 1%, TF, ROHS | VENKEL | CR0805-8W-1002FT(PbFREE) |
| H2512-04R99-1/8W1-T | 2 | ea | R14, R16 | RES, SMD, 0805, 4.99Ω, 1/8W, 1%, TF, ROHS | YAGEO | RC0805FR-074R99L |
| H2512-DNP | 0 | ea | R32, R33 | RES, SMD, 0805, DNP-PLACEHOLDER, ROHS | | |
| H2513-01000-1/4W1-T | 1 | ea | R45 | RES, SMD, 1206, 100Ω, 1/4W, 1%, TF, ROHS | STACKPOLE/FCI | RMC1/8 100R 1% T/R |
| H2513-01001-1/4W1-T | 1 | ea | R148 | RES, SMD, 1206, 1.00k, 1/1%, 4W, TF, ROHS | YAGEO | RC1206FR-071KL |
| H2515-01501-1W5-T | 4 | ea | R10, R11, R20, R22 | RES, SMD, 2512, 1.5k, 1W, 5%, TF, ROHS | VISHAY/DALE | CRCW25121K50JNEG |
| G108092LF | 1 | ea | T1 | TRANSFORMER-PWR, CUSTOM, 3.2µH, 20%, TH, 16P, 46X45, ROHS | GCI TECHNOLOGIES | G108092LF |
| P0544NL | 1 | ea | T3 | TRANSFORMER-GATE DRIVE, SMD, 8P, 9X8.6, 8P, 3950µH, ROHS | PULSE | P0544NL |
| P0584NL | 1 | ea | T6 | TRANSFORMER-GATE DRIVE, TH, 6P, 450µH, 1:1:1RATIO, ROHS | PULSE | P0584NL |
| P8205NL-T | 2 | ea | T2, T4 | TRANSFORMER-CURRENT SENSE, SMD, 8P, 500µH, 10A, ROHS | PULSE | P8205NL |
| 61215-3B-02500G | 2 | ea | HS1, HS2 | (SEE ASSEMBLY INSTRUCTIONS) HEATSINK-BLACK ANODIZED, 2.5, CUSTOM CUT, ROHS | AAVID/FCI | 61215-3B-02500G |

## Bill of Materials (Continued)

| PART NUMBER | QTY | UNITS | REFERENCE DESIGNATOR | DESCRIPTION | MANUFACTURER | MANUFACTURER PART |
|---|---|---|---|---|---|---|
| ISL6752DBEVAL1ZFG | 1 | ea | BAG & SHIP W/BOARD | PWBFG, ISL6752DBEVAL1Z, ROHS | INTERSIL | ISL6752DBEVAL1ZFG |
| ISL6754DBEVAL1ZFG | 1 | ea | BAG & SHIP W/BOARD | PWBFG, ISL6754DBEVAL1Z, ROHS | INTERSIL | ISL6754DBEVAL1ZFG |
| KPA8CTP | 2 | ea | P103, P104 | HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG & SCREW, ROHS | BERG/FCI | KPA8CTP |
| 10X12-STATIC-BAG | 1 | ea | Place assy in bag | BAG, STATIC, 10X12, ZIP | INTERSIL | 212403-015 |
| BP100-0.005-00-1112-NA | 2 | ea | HS1, HS2 (SEE ASSEMBLY INSTRUCTIONS) | INSULATION-BOND-PLY 5mil ADHESIVE TAPE, ROHS | BERGQUIST | BP100-0.005-00-1112-NA |
| LABEL-SERIAL NUMBER | 1 | ea | | LABEL-FOR SERIAL NUMBER AND BOM REV # | INTERSIL | LABEL-SERIAL NUMBER |

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